GSV1172

MIPI/LVDS to DisplayPort 1.2/ HDMI 1.4 Converter with Embedded MCU

May, 2024

Preliminary Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I²C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
AUX	AUX_CH, DisplayPort Auxiliary Channel
DPCD	DisplayPort Configuration Data
Main-Link	Unidirectional channel stream from DPTX to DPRX
SDP	Secondary-data Packet
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DP	DisplayPort (VESA)
DPRX	DisplayPort Receiver
DPTX	DisplayPort Transmitter
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	DisplayPort High Bit Rate, HDMI High Bit-Rate Audio
MST	DisplayPort Multi-Stream Transport
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV1172 is a high-performance, low-power MIPI D-PHY CSI-2/DSI and LVDS VESA/JEIDA to DisplayPort 1.2/HDMI 1.4 converter. With Single Port MIPI interface, 4K30 RGB can be transmitted using single port MIPI interface. For LVDS VESA/JEIDA interface, 1080p60 RGB can be transmitted using single port LVDS interface. By integrating enhanced microcontroller, GSV1172 has created a cost-effective solution that provides time-to-market advantages. The DisplayPort Transmitter supports up to 21.6Gbps (HBR2, 4-lane), HDMI Transmitter supports up to 9Gbps (TMDS, 3G/3Lane). The superior architecture of GSV1172 provides economical smaller footprint solutions using QFN64, targeting for low power embedded applications.

HDCP 1.4 is implemented in GSV1172 for its HDMI/DisplayPort output. Color Space Conversion, 420-444/422 Conversion, De-Interlacer and Downscaler are supported for flexible video processing. Audio Insertion of HDMI/DisplayPort Tx is supported in GSV1172 for audio processing.

Within 8kV HBM tolerance, GSV1172's operation temperature range is -40 ºC to 85 ºC.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 1.4 bandwidth, such as 4K@30Hz, 1080P@60Hz, 480i@60Hz.

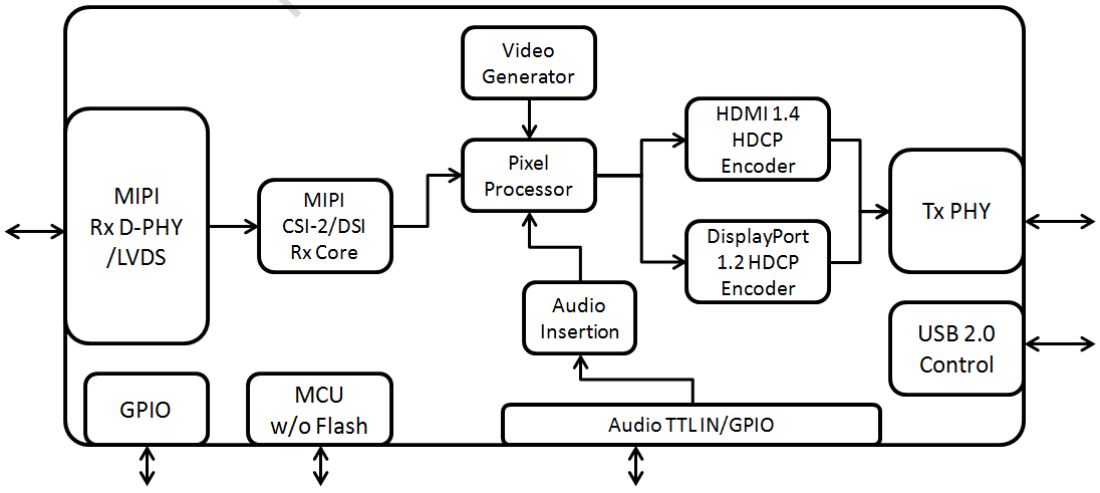


Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 HDMI Transmitter Features

- Compliant with HDMI 1.4b
- Compliant with HDCP 1.4
- Data rate up to 9Gbps (TMDS 3Gbps/3 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS input/output
- Support Color Space Converter in TMDS mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.2 DisplayPort Transmitter

- Compliant with VESA DisplayPort 1.2a
- Compliant with HDCP 1.4
- Support HBR2, HBR and RBR (5.4/2.7/1.62 Gbps)
- Flexible 1/2/4 lane Main-Link configuration
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Audio Insertion
- Support Spread Spectrum Clock (SSC)
- 3D format support of stacked frame, side-by-side, top-to-bottom

1.2.3 MIPI CSI-2/DSI-2 Receiver

- Support MIPI CSI-2 v3.0 version receiving using D-PHY interface
- Support MIPI DSI-2 v2.0 version receiving using D-PHY interface
- Support 2.5G bps 1/2/3/4-lane MIPI D-PHY Input
- CSI-2/DSI-2 Lane Reassignment and Polarity Flip
- Support RGB888, RGB666, RGB565, RGB555, RGB444
- Support YUV 4:2:2 8-bit, 10-bit, 12-bit
- Support YUV 4:2:0 legacy 8-bit
- Support burst and non-burst mode

1.2.4 Single-Port LVDS Receiver

- Compatible with VESA and JEIDA standards
  - Single -Port LVDS Receiver
  - Data rate up to 1.5Gbps per lane

1.2.5 Pixel Processor

- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with fixed horizontal and vertical 2 ratio for 4K to 2K conversion
- Deinterlacer for interlaced timing

1.2.6 Audio Input

- I2S and SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Insertion

1.2.7 System Features

- Optional External MCU (via I2C)/ Internal MCU mode
- Embedded MCU using External Flash
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO control from embedded MCU
- Mailbox feature for external MCU access on chip function status
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 MIPI/LVDS In to HDMI Out Application

TxPort is configured as HDMI 1.4 Output. This mode is designed for SoC MIPI/LVDS to HDMI 1.4 front-end interconnection. SoC can stream out a fixed timing via MIPI, and stream I2S audio to generate HDMI output by GSV1172.

With internal Color Space Converter, De-Interlacer, HDMI 1.4 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

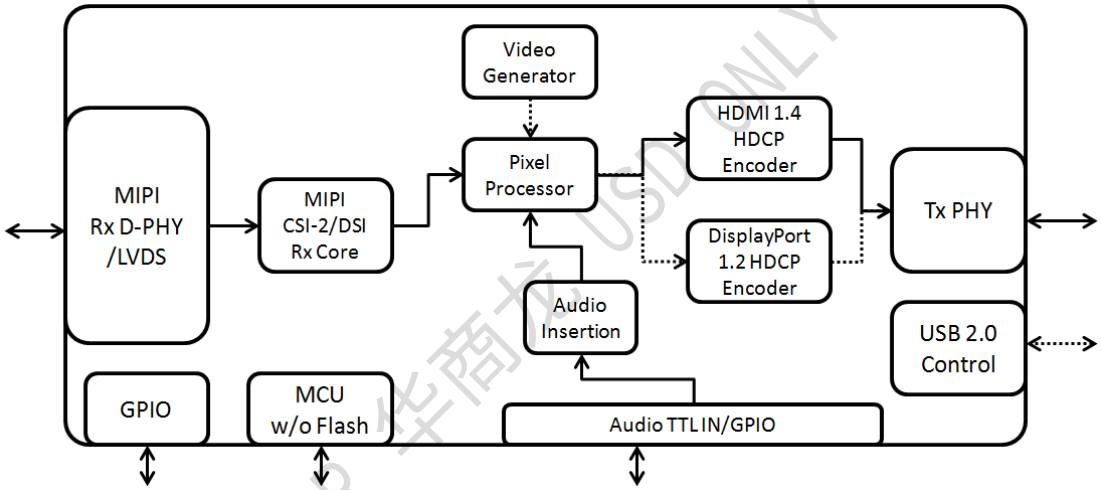


Figure 2. MIPI In to HDMI Out Application

1.3.2 MIPI/LVDS In to DisplayPort Out Application

TxPort is configured as DisplayPort 1.2 Output. This mode is designed for SoC MIPI/LVDS to DisplayPort 1.2 front-end interconnection. SoC can stream out a fixed timing via MIPI, and stream I2S audio to generate DisplayPort output by GSV1172.

With internal Color Space Converter, De-Interlacer, DisplayPort 1.2 output timing can be converted to any color space of RGB/YCbCr444/YCbCr422/YCbCr420. With Downscaler in Pixel Processor, output can be downscaled automatically when video stream bandwidth exceeds downstream capability.

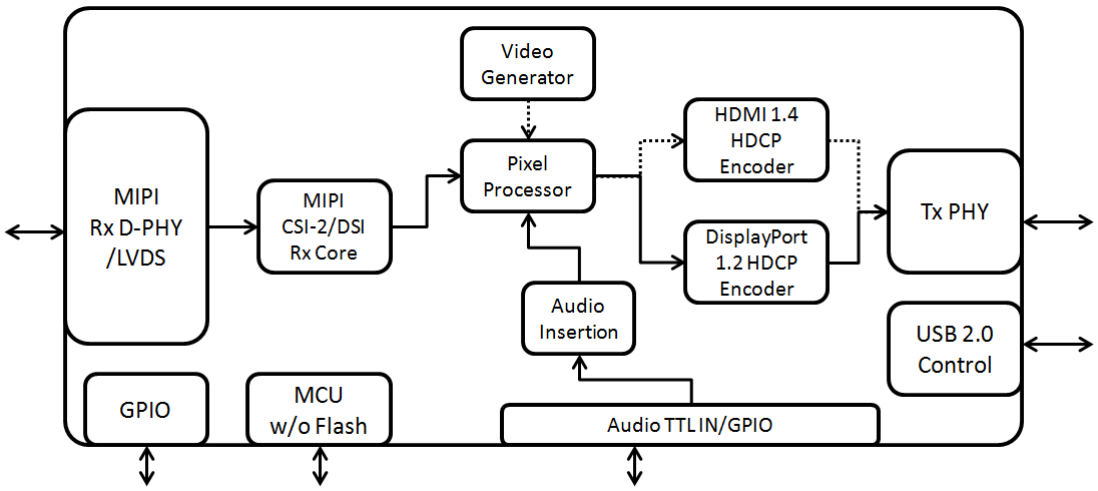


Figure 3. MIPI In to DisplayPort Out Application

1.4 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV1172 can detect Sampling Frequency and automatically update it in Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software. General application modes are listed below.

Table 2. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 3. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 4. 6-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D1	SDATA[1]	Input	I2S Data, 3/4 channels
AUD_D2	SDATA[2]	Input	I2S Data, 5/6 channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)

SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

2. Pin Description

2.1 Pin Diagram

QFN64 Pin definition is defined as below.

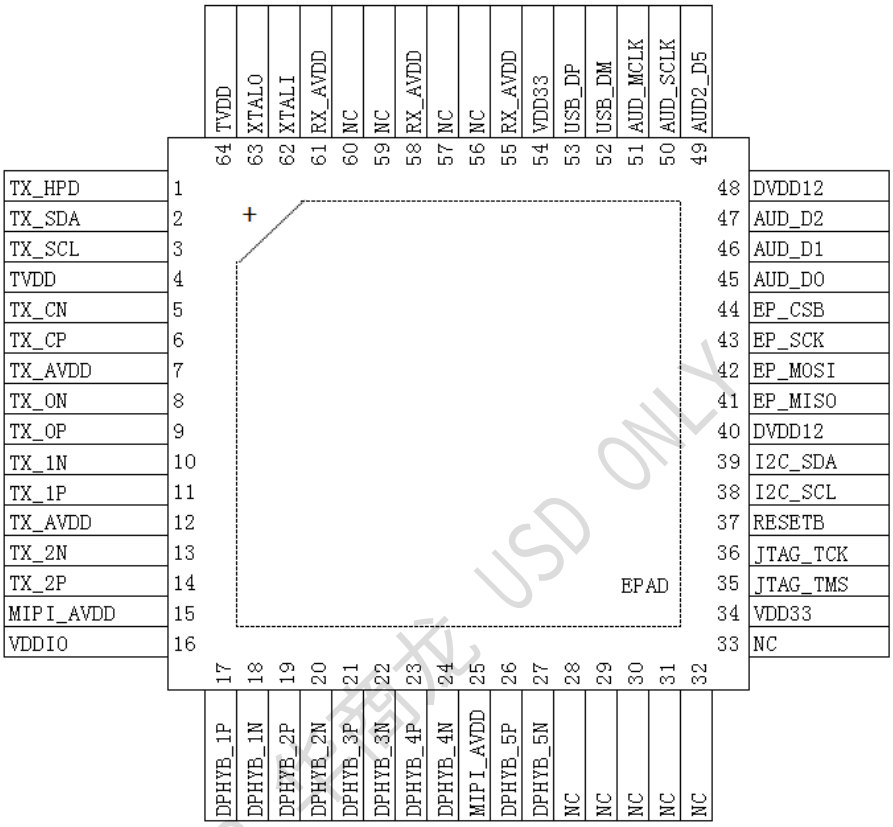


Figure 4. GSV1172 QFN64 Pin Diagram

2.2 QFN64 Pin Description

Table 5. QFN64 Pin Description

Pin Name	Direction	Pin No.	Description
HDMI/DisplayPort TX Pins			
TX_SDA	I/O	2	HDMI: TXA DDC SDA PAD DP: TXA AUX_P PAD
TX_SCL	O	3	HDMI: TXA DDC SCL PAD DP: TXA AUX_N PAD
TX_HPD	I	1	HDMI: TXA HPD PAD DP: TXA HPD PAD
TX_CN	O	5	HDMI: TXA Negative TMDS clock differential output DP: TXA Negative Main-Link differential data output [3]

TX_CP	O	6	HDMI: TXA Positive TMDS clock differential output DP: TXA Positive Main-Link differential data output [3]
TX_0N	O	8	HDMI: TXA Negative TMDS differential data output [0] DP: TXA Negative Main-Link differential data output [2]
TX_0P	O	9	HDMI: TXA Positive TMDS differential data output [0] DP: TXA Positive Main-Link differential data output [2]
TX_1N	O	10	HDMI: TXA Negative TMDS differential data output [1] DP: TXA Negative Main-Link differential data output [1]
TX_1P	O	11	HDMI: TXA Positive TMDS differential data output [1] DP: TXA Positive Main-Link differential data output [1]
TX_2N	O	13	HDMI: TXA Negative TMDS differential data output [2] DP: TXA Negative Main-Link differential data output [0]
TX_2P	O	14	HDMI: TXA Positive TMDS differential data output [2] DP: TXA Positive Main-Link differential data output [0]
Power/Ground Pins			
DVDD12	Power	40,48	Digital 1.2V voltage power supply
VDDIO	Power	16	Digital IO 3.3V voltage power supply
VDD33	Power	34,54, 64	Analog/Digital 3.3V voltage power supply
TVDD	Power	4	Analog 3.3V voltage power supply for TX Port
RX_AVDD	Power	55,58, 61	Analog 1.2V voltage power supply for RX Port
TX_AVDD	Power	7,12	Analog 1.2V voltage power supply for TX Port
MIPI_AVDD	Power	15,25	Analog 1.2V voltage power supply for Parallel Port
MIPI Tx Pins			
MIPIB_1P	I	17	MIPI: PORTB D-PHY Data[0] differential positive input Alternate: Digital IO PAD as GPIO0
MIPIB_1N	I	18	MIPI: PORTB D-PHY Data[0] differential negative input Alternate: Digital IO PAD as GPIO1
MIPIB_2P	I	19	MIPI: PORTB D-PHY Data[1] differential positive input Alternate: Digital IO PAD as GPIO2
MIPIB_2N	I	20	MIPI: PORTB D-PHY Data[1] differential negative input Alternate: Digital IO PAD as GPIO3
MIPIB_3P	I	21	MIPI: PORTB D-PHY clock differential positive input Alternate: Digital IO PAD as GPIO4
MIPIB_3N	I	22	MIPI: PORTB D-PHY clock differential negative input Alternate: Digital IO PAD as GPIO5

MIPIB_4P	I	23	MIPI: PORTB D-PHY Data[2] differential positive input Alternate: Digital IO PAD as GPIO6
MIPIB_4N	I	24	MIPI: PORTB D-PHY Data[2] differential negative input Alternate: Digital IO PAD as GPIO7
MIPIB_5P	I	26	MIPI: PORTB D-PHY Data[3] differential positive input Alternate: Digital IO PAD as GPIO10
MIPIB_5N	I	27	MIPI: PORTB D-PHY Data[3] differential negative input Alternate: Digital IO PAD as GPIO11
Not Connected Pins			
NC	I/O	28,29, 30,31, 32,33, 56,57, 59,60,	Not Connected Pins
Digital pins			
I2C_SDA	I/O	39	Default: Digital IO for I2C Data Alternate: GPIO8 for internal MCU
I2C_SCL	I/O	38	Default: Digital IO for I2C Clock Alternate: GPIO9 for internal MCU
AUD_SCLK	I/O	50	Digital IO PAD Default: SCLK of Audio Bus 2 Alternate 1: GPIO5 for internal MCU control Alternate 2: ADV_TIM2 for internal MCU control
AUD_MCLK	I/O	51	Digital IO PAD Default: MCLK of Audio Bus 2 Alternate 1: GPIO4 for internal MCU control Alternate 2: ADV_TIM1 for internal MCU control
AUD_D0	I/O	45	Digital IO PAD Default: Data0 of Audio Bus 2 Alternate 1: GPIO7 for internal MCU control Alternate 2: UART_TX for internal MCU control
AUD_D1	I/O	46	Digital IO PAD Default: Data1of Audio Bus 2 Alternate 1: GPIO10 for internal MCU control Alternate 2: UART_TX for internal MCU control

AUD_D2	I/O	47	Digital IO PAD Default: Data2 of Audio Bus 2 Alternate 1: GPIO11 for internal MCU control Alternate 2: UART_RX for internal MCU control
AUD_D5	I/O	49	Digital IO PAD Default: Data5 of Audio Bus 2 Alternate 1: GPIO6 for internal MCU control Alternate 2: UART_RX for internal MCU control Alternate 3: CEC
RESETB	I	37	Reset Pin. Low for reset state, High for functional state.
XTALI	I/O	62	25M Crystal Input
XTALO	I/O	63	25M Crystal output
JTAG_TMS	I/O	35	Default: TMS, Internal MCU programming pin Alternate: General Interrupt Output Pin
JTAG_TCK	I	36	Default: TCK, Internal MCU programming pin Alternate: AVMUTE Interrupt Output Pin
EP_SCK	I/O	43	Digital IO PAD Default: EP_SCK for internal MCU SPI control
EP_CSB	I/O	44	Digital IO PAD Default: EP_CSB for internal MCU SPI control
EP_MISO	I/O	41	Digital IO PAD Default: EP_MISO for internal MCU SPI control
EP_MOSI	I/O	42	Digital IO PAD Default: EP_MOSI for internal MCU SPI control
USB_DP	I/O	53	USB 2.0 D+ Pin
USB_DM	I/O	52	USB 2.0 D- Pin

3. Electrical Specifications

3.1 Timing Information

3.1.1 Power Up and Reset Timing Diagrams

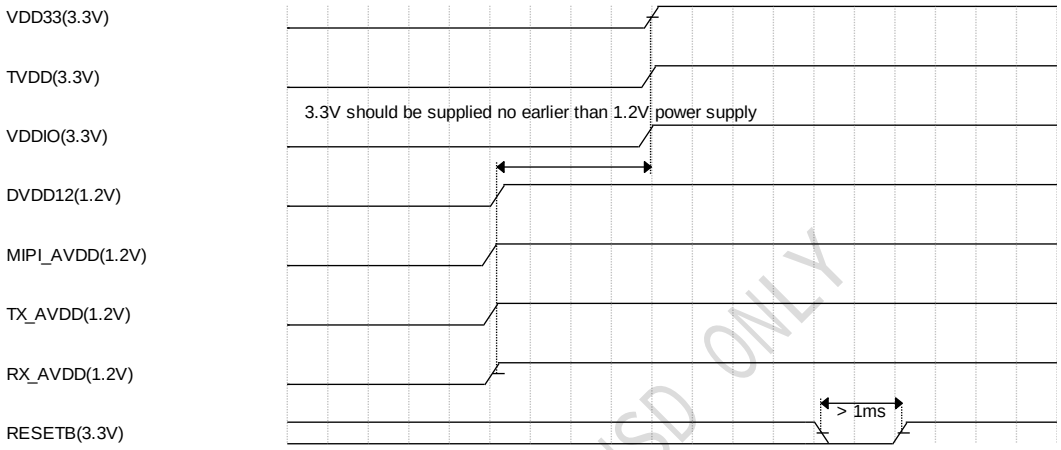


Figure 5. Power Up Sequence

3.1.2 I2C Timing Diagrams

The I2C bus uses 8-bit page address and 16-bit register address. ACK should be provided per 8-bit transaction. For every register, 8-bit data will be accessed. The device address is 0xB0 in 8-bit.

The I2C write timing is shown below.

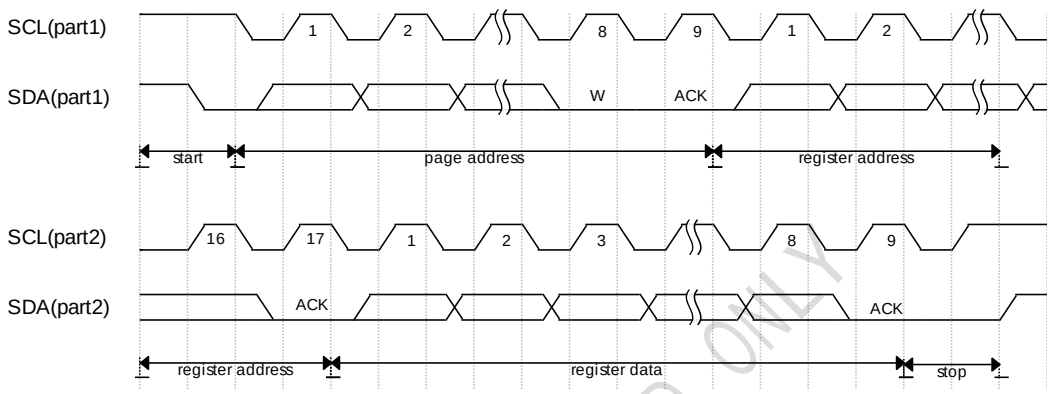


Figure 6. I2C Timing Diagram(Write)

The I2C read timing is shown below.

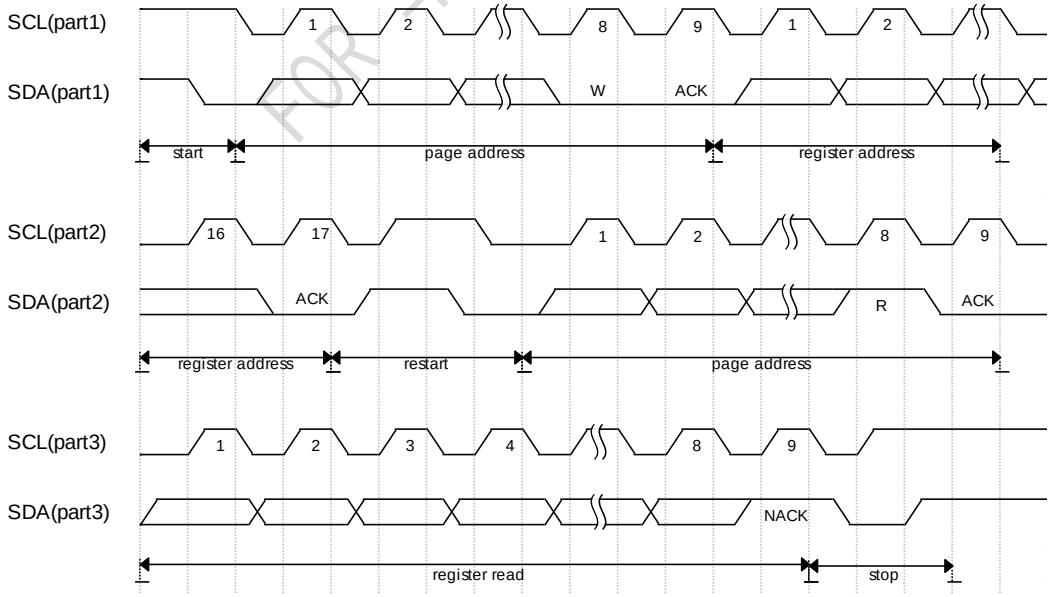


Figure 7. I2C Timing Diagram(Read)

3.2 Operating Conditions

3.2.1 Temperature Conditions

GSV1172's operation temperature range is -40 ºC to 85 ºC. The maximum junction temperature is at 125 ºC.

3.2.2 Audio Pin Conditions

GSV1172's Audio TTL pins can tolerate 2.8V~3.6V as logic HIGH.

3.2.3 I2C and SPI Conditions

GSV1172's I2C maximum SCL frequency is 400KHz.

Table 6. Recommended SPI Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_C	Serial Clock Frequency	12.5MHz		25	MHz
t_{CLH}	Serial Clock High Time	18	20	40.11	ns
t_{CKL}	Clock low-level width for QSPI	18	20	38.89	ns
t_{CLCH}	Serial Clock Rise Time	0.2	0.63		V/ns
t_{CHCL}	Serial Clock Fall Time	0.2	0.66		V/ns
t_{SLCH}	CS# Active Setup Time	5	60		ns
t_{CHSH}	CS# Active Hold Time	5	104		ns
t_{SHCH}	CS# Not Active Setup Time	5			ns
t_{CHSL}	CS# Not Active Hold Time	5			ns
t_{SHSL}	CS# High Time (Read/Write)	20	98		ns
t_{CLQX}	Output Hold Time	1.2	1.399		ns
t_{DVCH}	Data In Setup Time	2	17		ns
t_{CHDX}	Data In Hold Time	2	22		ns
t_{HLCH}	HOLD# Low Setup Time (Relative To Clock)	5			ns
t_{HHCH}	HOLD# High Setup Time (Relative To Clock)	5			ns

t_{CHHL}	HOLD# High Hold Time (Relative To Clock)	5			ns
t_{CHHH}	HOLD# Low Hold Time (Relative To Clock)	5			ns
t_{HLQZ}	HOLD# Low To High-Z Output			6	ns
t_{HHQX}	HOLD# High To Low-Z Output			6	ns
t_{CLQV}	Clock Low To Output Valid		4.999	7	ns

Table 7. Recommended I2C Timing Conditions

Symbol	Description	MIN.	TYP.	MAX.	Unit
f_{scl}	Clock Cycle for QSPI		300	400	KHz
t_{LOW}	clock low period	1.3	2		us
t_{HIGH}	clock high period	0.6	0.9		us
t_{BUF}	bus free time before new start	1.3			us
$t_{VD:DAT}$	data valid time			0.9	us
$t_{SU:STO}$	set-up time for stop condition	0.6	0.65		us
$t_{HD:DAT}$	data in hold time	0	1		us
$t_{SU:DAT}$	data in setup time	0.1	0.639		us
t_R	rise time		260	300	ns
t_F	fall time		20	300	ns

3.2.4 Absolute Maximum Ratings

Table 8. Absolute Maximum Ratings

PARAMETER	SYMBOL	VALUE	UNIT
Digital power supply	DVDD12	-0.3 to 1.4	V
Interface power supply	VDDIO	-0.3 to 4	V
Analog power supply(RX_AVDD,MIPI_AVDD)	AVDD	-0.3 to 1.4	V
Digital IO power supply	VDD33	-0.3 to 4	V
Operating Temperature Range	To	-40 to +85	℃
Storage Temperature Range	Tstg	-40 to +125	℃
Junction Temperature	Tj	+125	℃

3.2.5 ESD Protection

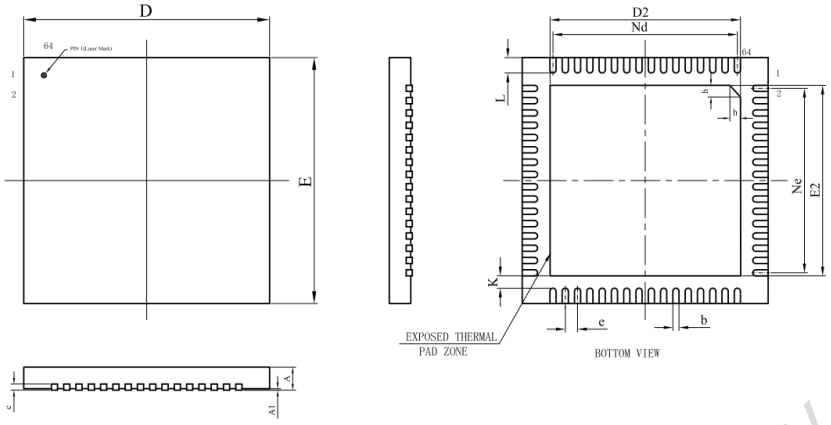
Table 9. ESD Protection

SYMBOL	PARAMETER	VALUE	UNIT

HBM	HBM for SIO(1) pins (JEDEC JS-001-2023)	8000	V
	HBM for other pins (JEDEC JS-001-2023)	4000	V
CDM	ESD CDM (JEDEC JS-002-2022)	1000	V
LU	Latch-up (JED78F)	200	mA

(1) SIO : Include DP Interface and MIPI interface pins.

4. Package Information



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	—	0.02	0.05
b	0.15	0.20	0.25
c	0.18	0.20	0.25
D	7.90	8.00	8.10
D2	6.10	6.20	6.30
e	0.40BSC		
Nd	6.00BSC		
E	7.90	8.00	8.10
E2	6.10	6.20	6.30
Ne	6.00BSC		
L	0.45	0.50	0.55
K	0.20	—	—
h	0.30	0.35	0.40
载体尺寸 (mil)	258*258		

Figure 8. Package Dimensions (QFN64)

5. Ordering Guide

Table 10. Ordering Information

Part Number.	Temperature Range	Package Description	Packing Type
GSV1172	-40°C to 85°C	QFN64	Tray

6. Revision History

Table 11. Revision history

Revision No.	Description	Date
V0.1	Draft Initial Version for internal review.	May 18, 2024
V0.2	Power Pin description update	Jun 27, 2024
V0.3	Remove SPI feature support from pin description	Sep 8, 2024
V0.4	Remove TypeC/DP support.	Sep 12, 2024
V0.5	Correct Temperature Range	Oct 9, 2024
V0.6	Unify temperature range of series chips	Nov 8, 2024
V0.7	Correct Typo of Package information	Nov 28, 2024
V0.8	Update I2C/SPI and I2S timing information	Dec 18, 2024
V0.9	Add Type-C/DisplayPort Support	Dec 30, 2024
V0.10	Remove Type-C Support again, only support DisplayPort	Jan 6, 2025

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