CC2340R5 SimpleLink™ *Bluetooth*® 5.3 Low Energy Wireless MCU

1 Features

Wireless microcontroller

- Powerful 48-MHz Arm® Cortex®-M0+ processor
- 512 KB of in-system programmable flash
- 12 KB of ROM for bootloader and drivers
- 36 KB of ultra-low leakage SRAM. Retained in standby mode
- 2.4 GHz RF transceiver compatible with Bluetooth® 5.3 Low Energy and IEEE 802.15.4 PHY and MAC
- Integrated Balun
- Supports over-the-air upgrade (OTA)

Low power consumption

- MCU consumption:
  - 2.6 mA active mode, CoreMark®
  - 56 µA/MHz running CoreMark®
  - 700 nA standby mode, RTC, 36 KB RAM
  - 150 nA shutdown mode, wake-up on pin
- Radio Consumption:
  - 5.3 mA RX
  - 5.0 mA TX at 0 dBm
  - < 12.0 mA TX at +8 dBm

Wireless protocol support

- *Bluetooth*® 5.3 Low Energy
- Zigbee®
- SimpleLink™ TI 15.4-stack
- Proprietary systems

High-performance radio

- -102 dBm for Bluetooth® Low Energy 125 Kb/s
- -96 dBm for Bluetooth® Low Energy 1 Mb/s
- Output power up to +8 dBm with temperature compensation

Regulatory compliance

- Suitable for systems targeting compliance with these standards:
  - EN 300 328 (Europe)
  - FCC CFR47 Part 15
  - ARIB STD-T66 (Japan)

MCU peripherals

- Up to 26 I/O Pads
  - 2 IO pads SWD, muxed with GPIOs
  - 2 IO pads LFXT, muxed with GPIOs
  - Up to 2215 DIOs (analog or digital IOs)
- Digital peripherals can be routed to any GPIO
- 3× 16-bit and 1× 24-bit general-purpose timers, Quadrature decode mode support
- 12-bit ADC, 1.2 Mbps with external reference, 260 kbps with internal reference, 12 external ADC inputs
- 1× low power comparator
- 1× UART
- 1× SPI
- 1× I^2C
- Real-time clock (RTC)
- Integrated temperature and battery monitor
- Watchdog timer

Security enablers

- AES 128-bit cryptographic accelerator
- Random number generator from on-chip analog noise

Development tools and software

- LP-EM-CC2340R5 LaunchPad Development Kit
- SimpleLink™ CC23xx Software Development Kit (SDK)
- SmartRF™ Studio for simple radio configuration
- SysConfig system configuration tool

Operating range

- On-chip buck DC/DC converter
- 1.71-V to 3.8-V single supply voltage
- -40 to +125°C (Ta = Tj = 125°C)

Package

- 5-mm × 5-mm RKP QFN40 (26 GPIOs)
- 4-mm × 4-mm RGE QFN24 (12 GPIOs)
- RoHS-compliant package

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2 Applications

- Medical
  - Home healthcare – blood glucose monitors, blood pressure monitor, CPAP machine, electronic thermometer
  - Patient monitoring & diagnostics – medical sensor patches
  - Personal care & Fitness – electric toothbrush, wearable fitness & activity monitor
- Building automation
  - Building security systems – motion detector, electronic smart lock, door and window sensor, garage door system, gateway
  - HVAC – thermostat, wireless environmental sensor
  - Fire safety system – smoke and heat detector
  - Video surveillance – IP network camera
- Lighting
  - LED luminaire
  - Lighting Control – daylight sensor, lighting sensor, wireless control
- Factory automation and control
- Retail automation & payment – Electronic point of sale
- Communication equipment
  - Wired networking – wireless LAN or Wi-Fi access points, edge router
- Personal electronics
  - Connected peripherals – consumer wireless module, pointing devices, keyboards and keypads
  - Gaming – electronic and robotic toys
  - Wearables (non-medical) – smart trackers, smart clothing

3 Description

The SimpleLink™ CC2340R5 device is a 2.4 GHz wireless microcontroller (MCU) targeting *Bluetooth*® 5.3 Low Energy, Zigbee®, IEEE 802.15.4, and Proprietary 2.4 GHz applications. The device is optimized for low-power wireless communication with on-chip dual image Over the Air Download (OAD) support in Building automation (wireless sensors, lighting control, beacons), asset tracking, medical, retail EPOS (electronic point of sale), ESL (electronic shelf label), and Personal electronics (toys, HID, stylus pens) markets. The highlighted features of this device include:

- Support for *Bluetooth* ® 5 features: LE Coded PHYs (Long Range), LE 2-Mbit PHY (High Speed), Advertising Extensions, Multiple Advertisement Sets, CSA#2, Direction Finding, as well as backwards compatibility and support for key features from the *Bluetooth* ® 4.2 and earlier Low Energy specifications.
- Fully-qualified *Bluetooth* ® 5.3 software protocol stack included with the SimpleLink™ CC23xx Software Development Kit (SDK).
- Support for Bluetooth® mesh (low power nodes).
- Zigbee® protocol stack support in the SimpleLink™ CC23x0Rx Software Development Kit (SDK).
- Ultra-low standby current of 0.7 µA with RTC operational and full RAM retention that enables significant battery life extension especially for applications with longer sleep intervals.
- Very low average radio currents for duty-cycled BLE use-cases. Average radio current ~6uA when operating in a Bluetooth®Low Energy connection with TX output power = 0dBm and 1s connection interval.
- Extended temperature support with lowest standby current of 11 µA at 105 ºC.
- Integrated BALUN for reduced Bill-of-Material (BOM) board layout
- Excellent radio sensitivity and robustness (selectivity and blocking) performance for *Bluetooth* ® Low Energy (-102 dBm for 125-Kbps LE Coded PHY, with integrated BALUN).

The CC2340R5 device is part of the SimpleLink™ MCU platform, which consists of Wi-Fi®, *Bluetooth* Low Energy, Thread, Zigbee, Sub-1 GHz MCUs, and host MCUs that all share a common, easy-to-use development environment with a single core software development kit (SDK) and rich tool set. A one-time integration of the SimpleLink™ platform enables you to add any combination of the portfolio's devices into your design, allowing 100 percent code reuse when your design requirements change. For more information, visit SimpleLink™ MCU platform.

Device Information

PART NUMBER(1)	PACKAGE	BODY SIZE (NOM)
CC2340R52E0RGER	QFN24	4.00 mm × 4.00 mm
CC2340R52E0RKPR	QFN40	5.00 mm × 5.00 mm

(1) For the most current part, package, and ordering information for all available devices, see the Package Option Addendum in Section 12, or see the TI website.

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4 Functional Block Diagram

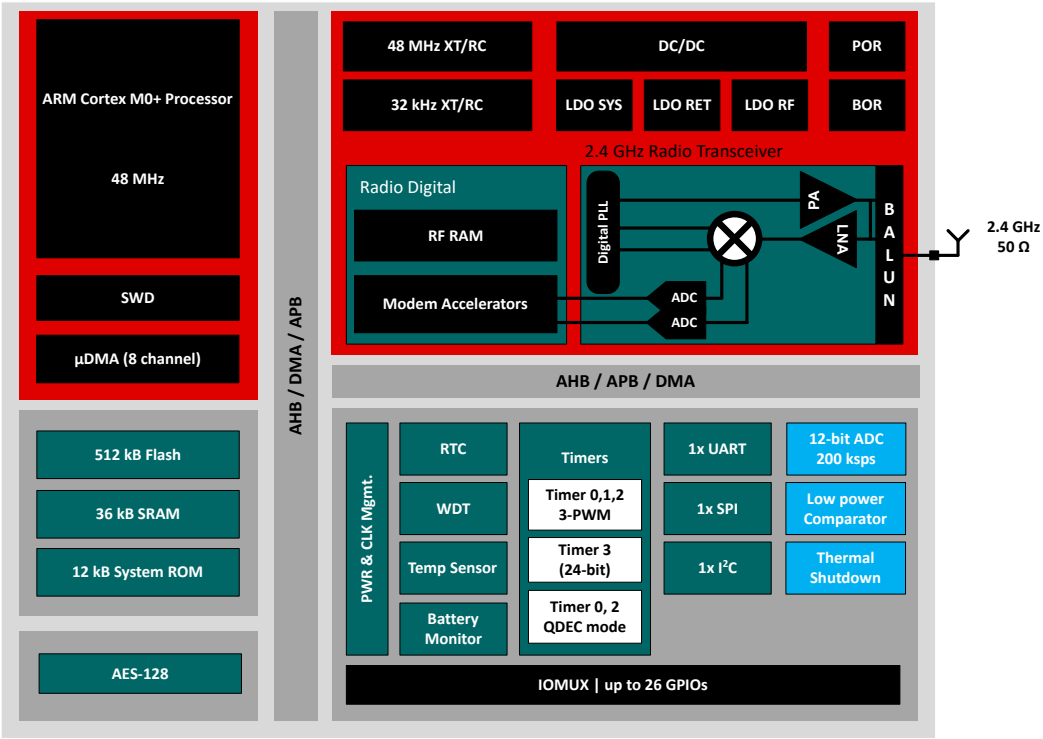

Figure 4-1. CC2340R5 Block Diagram

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
February 2022	*	Initial Release

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6 Device Comparison

Device	RADIO SUPPORT										FLASH (KB)	RAM + Cache (KB)	GPIO	PACKAGE SIZE				
	Sub-1 GHz Prop.	2.4GHz Prop.	Wireless M-Bus	Wi-SUN®	Sidewalk	*Bluetooth*® LE	ZigBee	Thread	Multiprotocol	+20 dBm PA				4 X 4 mm VQFN (24)	4 X 4 mm VQFN (32)	5 X 5 mm VQFN (32)	5 X 5 mm VQFN (40)	7 X 7 mm VQFN (48)
CC1310	X		X								32-128	16-20 + 8	10-30		X	X		X
CC1311R3	X		X								352	32 + 8	22-30				X	X
CC1311P3	X		X							X	352	32 + 8	26					X
CC1312R	X		X	X							352	80 + 8	30					X
CC1312R7	X		X	X	X				X		704	144 + 8	30					X
CC1352R	X	X	X	X		X	X	X	X		352	80 + 8	28					X
CC1352P	X	X	X	X		X	X	X	X	X	352	80 + 8	26					X
CC1352P7	X	X	X	X	X	X	X	X	X	X	704	144 + 8	26	X				X
CC2340R2						X	X	X	X		256	28	12	X			X	
CC2340R5						X	X	X			512	36	12-26			X		
CC2340R5-Q1						X	X	X	X		512	36	19		X			
CC2640R2F						X					128	20 + 8	10-31		X	X		X
CC2642R						X					352	80 + 8	31					X
CC2642R-Q1						X					352	80 + 8	31					X
CC2651R3		X				X	X				352	32 + 8	23-31				X	X
CC2651P3		X				X	X			X	352	32 + 8	22-26				X	X
CC2652R		X				X	X	X	X		352	80 + 8	31					X
CC2652RB		X				X	X	X	X		352	80 + 8	31					X
CC2652R7		X				X	X	X	X		704	144 + 8	31					X
CC2652P		X				X	X	X	X	X	352	80 + 8	26					X
CC2652P7		X				X	X	X	X	X	704	144 + 8	26					X

7 Pin Configuration and Functions

7.1 Pin Diagram – RKP Package (Top View)

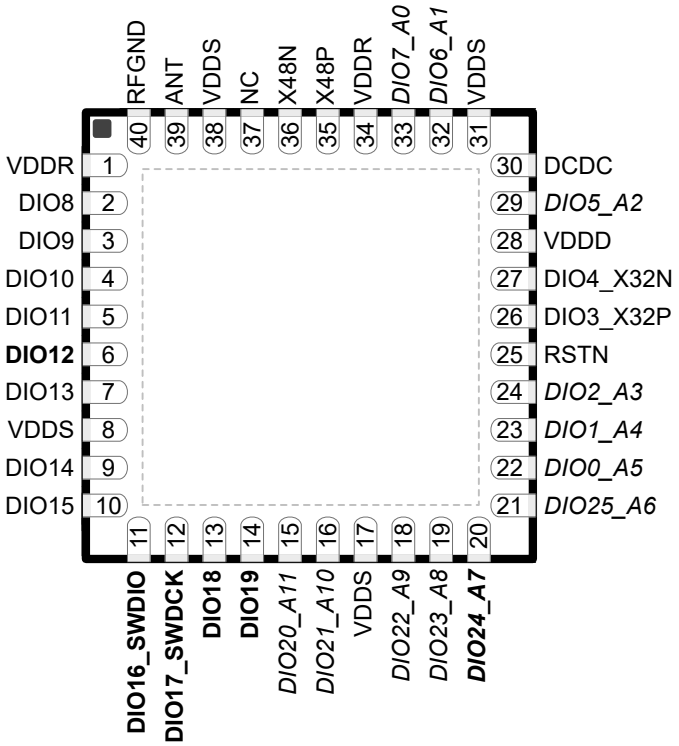

Figure 7-1. RKP (5-mm × 5-mm) Pinout, 0.4-mm Pitch (Top View)

The following I/O pins marked in Figure 7-1 in **bold** have high-drive capabilities:

- Pin 6, DIO12
- Pin 11, DIO16_SWDIO
- Pin 12, DIO17_SWDCK
- Pin 13, DIO18
- Pin 14, DIO19
- Pin 20, DIO24_A7

The following I/O pins marked in Figure 7-1 in *italics* have analog capabilities:

- Pin 15, DIO20_A11
- Pin 16, DIO21_A10
- Pin 18, DIO22_A9
- Pin 19, DIO23_A8
- Pin 20, DIO24_A7
- Pin 21, DIO25_A6
- Pin 22, DIO0_A5
- Pin 23, DIO1_A4
- Pin 24, DIO2_A3
- Pin 29, DIO5_A2
- Pin 32, DIO6, A1
- Pin 33, DIO7_A0

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7.2 Signal Descriptions – RKP Package

Table 7-1. Signal Descriptions – RKP Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
EGP	—	—	GND	Ground – exposed ground pad(1)
VDDR	1	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (3) (4)
DIO8	2	I/O	Digital	GPIO
DIO9	3	I/O	Digital	GPIO
DIO10	4	I/O	Digital	GPIO
DIO11	5	I/O	Digital	GPIO
DIO12	6	I/O	Digital	GPIO, high-drive capability
DIO13	7	I/O	Digital	GPIO
VDDS	8	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO14	9	I/O	Digital	GPIO
DIO15	10	I/O	Digital	GPIO
DIO16_SWDIO	11	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO17_SWDCK	12	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO18	13	I/O	Digital	GPIO, high-drive capability
DIO19	14	I/O	Digital	GPIO, high-drive capability
DIO20_A11	15	I/O	Digital or Analog	GPIO, analog capability
DIO21_A10	16	I/O	Digital or Analog	GPIO, analog capability
VDDS	17	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO22_A9	18	I/O	Digital or Analog	GPIO, analog capability
DIO23_A8	19	I/O	Digital or Analog	GPIO, analog capability
DIO24_A7	20	I/O	Digital or Analog	GPIO, Analog capability, high-drive capability
DIO25_A6	21	I/O	Digital or Analog	GPIO, analog capability
DIO0_A5	22	I/O	Digital or Analog	GPIO, analog capability
DIO1_A4	23	I/O	Digital or Analog	GPIO, analog capability
DIO2_A3	24	I/O	Digital or Analog	GPIO, analog capability
RSTN	25	I	Digital	Reset, active low. No internal pullup resistor
DIO3_X32P	26	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 1, Optional TCXO input
DIO4_X32N	27	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 2
VDDD	28	—	Power	For decoupling of internal 1.28-V regulated core-supply. Connect an external 1 µF decoupling capacitor.(2)
DIO5_A2	29	I/O	Digital or Analog	GPIO, analog capability
DCDC	30	—	Power	Switching node of internal DC/DC converter(5)
VDDS	31	—	Power	1.71-V to 3.8-V analog supply(5)
DIO6_A1	32	I/O	Digital or Analog	GPIO, analog capability
DIO7_A0	33	I/O	Digital or Analog	GPIO, analog capability
NC	34	—	—	No Connect
VDDR	35	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(2) (3) (4)
X48P	36	—	Analog	48-MHz crystal oscillator pin 1
X48N	37	—	Analog	48-MHz crystal oscillator pin 2
VDDS	38	—	Power	1.71-V to 3.8-V analog supply(5)
ANT	39	I/O	RF	2.4 GHz TX, RX

Table 7-1. Signal Descriptions – RKP Package (continued)

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
RFGND	40	—	RFGND	RF Ground

(1) EPG is the only non-RF ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(2) Do not supply external circuitry from this pin.
(3) VDDR pins 1 and 35 must be tied together on the PCB.
(4) Output from internal DC/DC and LDO is trimmed to 1.5 V.
(5) For more details, see the technical reference manual listed in Section 11.2.

7.3 Connections for Unused Pins and Modules – RKP Package

Table 7-2. Connections for Unused Pins – RKP Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	2–7 9–10 13–14	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	11	NC, GND, or VDDS	GND or VDDS
	DIO17_SWDCK	12	NC, GND, or VDDS	GND or VDDS
GPIO (digital or analog)	DIOn_Am	15–16 18–24 29 32–33	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	26	NC or GND	NC
	DIO4_X32N	27		
DC/DC converter(2)	DCDC	30	NC	NC
	VDDS	8, 17, 31, 38	VDDS	VDDS

(1) NC = No connect
(2) When the DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF DCDC capacitor must be kept on the VDDR net.

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7.4 Pin Diagram – RGE Package (Top View)

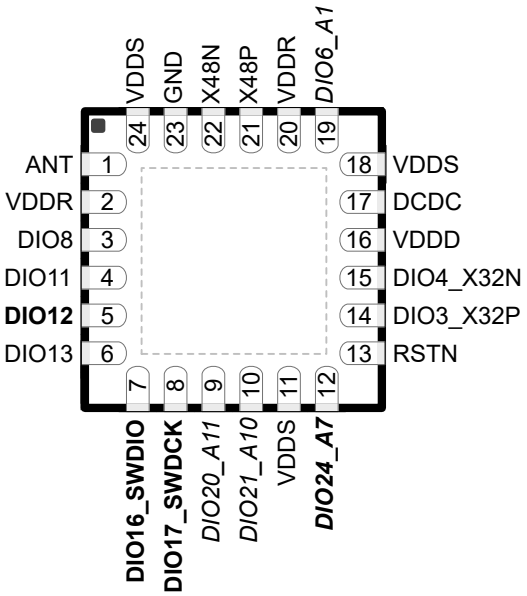

Figure 7-2. RGE (4-mm × 4-mm) Pinout, 0.4-mm Pitch (Top View)

The following I/O pins marked in Figure 7-2 in **bold** have high-drive capabilities:

- Pin 5, DIO12
- Pin 7, DIO16_SWDIO
- Pin 8, DIO17_SWDCK
- Pin 12, DIO24_A7

The following I/O pins marked in Figure 7-2 in *italics* have analog capabilities:

- Pin 9, DIO20_A11
- Pin 10, DIO21_A10
- Pin 12, DIO24_A7
- Pin 19, DIO6, A1

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7.5 Signal Descriptions – RGE Package

Table 7-3. Signal Descriptions – RGE Package

PIN		I/O	TYPE	DESCRIPTION
NAME	NO.			
EGP	—	—	GND	Ground – exposed ground pad(1)
ANT	1	I/O	RF	2.4 GHz TX, RX
VDDR	2	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO(2) (3) (4)
DIO8	3	I/O	Digital	GPIO
DIO11	4	I/O	Digital	GPIO
DIO12	5	I/O	Digital	GPIO, high-drive capability
DIO13	6	I/O	Digital	GPIO
DIO16_SWDIO	7	I/O	Digital	GPIO, SWD interface: mode select or SWDIO, high-drive capability
DIO17_SWDCK	8	I/O	Digital	GPIO, SWD interface: clock, high-drive capability
DIO20_A11	9	I/O	Digital or Analog	GPIO, analog capability
DIO21_A10	10	I/O	Digital or Analog	GPIO, analog capability
VDDS	11	—	Power	1.71-V to 3.8-V DIO supply(5)
DIO24_A7	12	I/O	Digital or Analog	GPIO, Analog capability, high-drive capability
RSTN	13	I	Digital	Reset, active low. No internal pullup resistor
DIO3_X32P	14	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 1, Optional TCXO input
DIO4_X32N	15	I/O	Digital or Analog	GPIO, 32-kHz crystal oscillator pin 2
VDDD	16	—	Power	For decoupling of internal 1.28-V regulated core-supply. Connect an external 1 µF decoupling capacitor.(2)
DCDC	17	—	Power	Switching node of internal DC/DC converter(5)
VDDS	18	—	Power	1.71-V to 3.8-V analog supply(5)
DIO6_A1	19	I/O	Digital or Analog	GPIO, analog capability
VDDR	20	—	Power	Internal supply, must be powered from the internal DC/DC converter or the internal LDO. Connect an external 10 µF decoupling capacitor.(2) (3) (4)
X48P	21	—	Analog	48-MHz crystal oscillator pin 1
X48N	22	—	Analog	48-MHz crystal oscillator pin 2
GND	23	—	GND	Ground
VDDS	24	—	Power	1.71-V to 3.8-V analog supply(5)

(1) EPG is the main ground connection for the device. Good electrical connection to device ground on printed circuit board (PCB) is imperative for proper device operation.
(2) Do not supply external circuitry from this pin.
(3) VDDR pins 2 and 20 must be tied together on the PCB.
(4) Output from internal DC/DC and LDO is trimmed to 1.5 V.
(5) For more details, see technical reference manual listed in Section 11.2.

7.6 Connections for Unused Pins and Modules – RGE Package

Table 7-4. Connections for Unused Pins – RGE Package

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital)	DIOn	3–6	NC, GND, or VDDS	NC
SWD	DIO16_SWDIO	7	NC, GND, or VDDS	GND or VDDS
	DIO17_SWDCK	8	NC, GND, or VDDS	GND or VDDS

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Table 7-4. Connections for Unused Pins – RGE Package (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER	ACCEPTABLE PRACTICE(1)	PREFERRED PRACTICE(1)
GPIO (digital or analog)	DIOn_Am	9–10 12 19	NC, GND, or VDDS	NC
32.768-kHz crystal	DIO3_X32P	14	NC or GND	NC
	DIO4_X32N	15		
DC/DC converter(2)	DCDC	17	NC	NC
	VDDS	11, 18, 24	VDDS	VDDS

(1) NC = No connect
(2) Whenthe DC/DC converter is not used, the inductor between DCDC and VDDR can be removed. VDDR must still be connected and the 10 µF DCDC capacitor must be kept on the VDDR net.

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7.7 RKP and RGE Peripheral Pin Mapping

Table 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
2	1	VDDR	VDDR	—	N/A	N/A
3	2	DIO8	GPIO8	I/O	0	I/O
			SPI0SCLK		1	I/O
			UART0RTS		2	O
			T1C0N		3	O
			I2C0SDA		4	I/O
			T0C0N		5	O
			DTB3		7	O
—	3	DIO9	GPIO9	I/O	0	I/O
			T3C0		1	O
			LRFD3		3	O
—	4	DIO10	GPIO10	I/O	0	I/O
			LPCO		1	O
			T2PE		2	O
			T3C0N		3	O
4	5	DIO11	GPIO11	I/O	0	I/O
			SPI0CSN		1	I/O
			T1C2N		2	O
			T0C0		3	O
			LRFD0		4	O
			SPI0MISO		5	I/O
			DTB9		7	O
5	6	DIO12	GPIO12	I/O	0	I/O
			SPI0MISO		1	I/O
			SPI0MOSI		2	I/O
			UART0RXD		3	I
			T1C1		4	O
			I2C0SDA		5	I/O
			DTB0		7	O
6	7	DIO13	GPIO13	I/O	0	I/O
			SPI0MISO		1	I/O
			SPI0MOSI		2	I/O
			UART0TXD		3	O
			T0C0N		4	O
			T1F		5	O
			DTB4		7	O
—	8	VDDS	VDDS	—	N/A	N/A
—	9	DIO14	DIO14	I/O	0	N/A
			T3C2		1	O
			T1C2N		2	O
			LRFD5		3	O
			T1F		4	O

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Table 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
—	10	DIO15	GPIO15	I/O	0	I/O
			UART0RXD		1	I
			T2C0N		2	O
			CKMIN		3	I
7	11	DIO16_SWDIO	GPIO16	I/O	0	I/O
			SPI0MOSI		1	I/O
			UART0RXD		2	I
			I2C0SDA		3	I/O
			T1C2		4	O
			T1C0N		5	O
8	12	DIO17_SWDCK	GPIO17	I/O	0	I/O
			SPI0SCLK		1	I/O
			UART0TXD		2	O
			I2C0SCL		3	I/O
			T1C1N		4	O
			T0C2		5	O
			DTB11		7	O
—	13	DIO18	GPIO18	I/O	0	I/O
			T3C0		1	O
			LPCO		2	O
			UART0TXD		3	O
			SPI0SCLK		4	I/O
			DTB12		7	O
—	14	DIO19	GPIO19	I/O	0	I/O
			T3C1		1	O
			T2PE		2	O
			SPI0MOSI		4	I/O
			DTB13		7	O
9	15	DIO20_A11	GPIO20	I/O	0	I/O
			LPCO		1	O
			UART0TXD		2	O
			UART0RXD		3	I
			T1C0		4	O
			SPI0MISO		5	I/O
			ADC11		6	I
			DTB1		7	O
10	16	DIO21_A10	GPIO21	I/O	0	I/O
			UART0CTS		1	I
			T1C1N		2	O
			T0C1		3	O
			SPI0MISO		4	I/O
			LRFD1		5	O
			ADC10/LPC+		6	I
			DTB2		7	O

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Table 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
11	17	VDDS	VDDS	—	N/A	N/A
—	18	DIO22_A9	GPIO22	I/O	0	I/O
			T2C0		1	O
			UART0RXD		2	I
			T3C1N		3	O
			ADC9		6	I
			DTB14		7	O
—	19	DIO23_A8	GPIO23	I/O	0	I/O
			T2C1		1	O
			T3C2N		3	O
			ADC8/LPC+/LPC-		6	I
12	20	DIO24_A7	GPIO24	I/O	0	I/O
			SPI0SCLK		1	I/O
			T1C0		2	O
			T3C0		3	O
			T0PE		4	O
			I2C0SCL		5	I/O
			ADC7/LPC+/LPC-		6	I
			DTB5		7	O
—	21	DIO25_A6	GPIO25	I/O	0	I/O
			SPI0MISO		1	I/O
			I2C0SCL		2	I/O
			T2C2N		3	O
			ADC6		6	I
—	22	DIO0_A5	GPIO0	I/O	0	I/O
			SPI0CSN		1	I/O
			I2C0SDA		2	I/O
			T3C2		3	O
			ADC5		6	I
—	23	DIO1_A4	GPIO1	I/O	0	I/O
			T3C1		1	O
			LRFD7		2	O
			T1F		3	O
			UART0RTS		4	O
			ADC4		5	I
			DTB15		6	O
—	24	DIO2_A3	GPIO2	I/O	0	I/O
			T0PE		1	O
			T2C1N		2	O
			UART0CTS		3	I
			ADC3		6	I
13	25	RTSN	RSTN	—	N/A	N/A

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Table 7-5. RKP (QFN40) and RGE (QFN24) Peripheral Pin Mapping (continued)

PIN NO.		PIN NAME	SIGNAL NAME	SIGNAL TYPE[1]	PIN MUX ENCODING	SIGNAL DIRECTION
QFN24	QFN40					
14	26	DIO3_X32P	GPIO3	I/O	0	I/O
			LFCI		1	I
			T0C1N		2	O
			LRFD0		3	O
			T3C1		4	O
			T1C2		5	O
			LFXT_P		6	I
			DTB7		7	O
15	27	DIO4_X32N	GPIO4		0	I/O
			T0C2N		1	O
			UART0TXD		2	O
			LRFD1		3	O
			SPI0MOSI		4	I/O
			T0C2		5	O
			LFXT_N		6	I
			DTB8		7	O
16	28	VDDD	VDDD	—	N/A	N/A
—	29	DIO5_A2	GPIO5	I/O	1	I/O
			T2C2		2	O
			LRFD6		3	O
			ADC2		6	I
17	30	DCDC	DCDC	—	N/A	N/A
18	31	VDDS	VDDS	—	N/A	N/A
19	32	DIO6_A1	GPIO6	I/O	0	I/O
			SPI0CSN		1	I/O
			I2C0SCL		2	I/O
			T1C2		3	O
			LRFD2		4	O
			UART0TXD		5	O
			ADC1/AREF+		6	I
			DTB6		7	O
—	33	DIO7_A0	GPIO7	I/O	0	I/O
			T3C1		1	O
			LRFD4		2	O
			ADC0/AREF-		6	I
20	34	VDDR	VDDR	—	N/A	N/A
21	35	X48P	X48P	—	N/A	N/A
22	36	X48N	X48N	—	N/A	N/A
—	37	NC	NC	—	N/A	N/A
24	38	VDDS	VDDS	—	N/A	N/A
1	39	ANT	ANT	—	N/A	N/A
—	40	RFGND	RFGND	—	N/A	N/A
	GND_TAB			—	N/A	N/A

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

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7.8 RKP and RGE Peripheral Signal Descriptions

Table 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descripitions

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
ADC	ADC11	9	15	I/O	I	HP ADC channel 11 input
	ADC10	10	16			HP ADC channel 10 input
	ADC9	—	18			HP ADC channel 9 input
	ADC8	—	19			HP ADC channel 8 input
	ADC7	12	20			HP ADC channel 7 input
	ADC6	—	21			ADC channel 6 input
	ADC5	—	22			ADC channel 5 input
	ADC4	—	23			ADC channel 4 input
	ADC3	—	24			ADC channel 3 input
	ADC2	—	29			ADC channel 2 input
	ADC1	19	32			HP ADC channel 1 input
	ADC0	—	33			HP ADC channel 0 input
ADC Reference	AREF+	19	32	I/O	I	ADC external voltage reference, positive terminal
	AREF-	—	33			ADC external voltage reference, negative terminal
Analog Test Bus	ATEST0	9	15	I/O	O	Analot test bus output 0
	ATEST1	10	16			Analog test bus output 1
	FLTP3	10	16	I/O	O	Flash testpad output 3
	FLTP1	13	25			Flashtestpad output 1
Clock	X32P	14	26	I/O	I	32-kHz crystal oscillator pin 1, Optional TCXO input
	X32N	15	27	I/O	I	32-kHz crystal oscillator pin 2
	X48P	21	35	—	I	48-MHz crystal oscillator pin 1
	X48N	22	36	—	I	48-MHz crystal oscillator pin 2
	CLKMIN	—	10	I/O	I	TDC or HFOSC tracking loop reference clock input
	LFCI	14	26	I/O	I	Low frequency clock input (LFXT bypass clock from pin)
Comparator	LPC0	—	4	I/O	O	Low power comparator output
		—	13			
		9	15			
Comparitor Input	LPC+	10	16	I/O	I	Low power comparator positive input terminal
		—	19			
		12	20			
	LPC-	—	19			Lower power comparator negative input terminal
		12	20			

Table 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descripitions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
Digital Test Bus	DTB3	3	2	I/O	O	Digital test bus output 3
	DTB9	4	5			Digital test bus output 9
	DTB0	5	6			Digital test bus output 0
	DTB4	6	7			Digital test bus output 4
	DTB10	7	11			Digital test bus output 10
	DTB11	8	12			Digital test bus output 11
	DTB12	—	13			Digital test bus output 12
	DTB13	—	14			Digital test bus output 13
	DTB1	9	15			Digital test bus output 1
	DTB2	10	16			Digital test bus output 2
	DTB14	—	18			Digital test bus output 14
	DTB5	12	20			Digital test bus output 5
	DTB15	—	23			Digitial test bus output 15
	DTB7	14	26			Digital test bus output 7
	DTB8	15	27			Digital test bus output 8
	DTB6	19	32			Digital test bus output 6
GPIO	GPIO8	3	2	I/O	I/O	General-purpose input or output
	GPIO9	—	3			
	GPIO10	—	4			
	GPIO11	4	5			
	GPIO12	5	6			
	GPIO13	6	7			
	GPIO14	—	9			
	GPIO15	—	10			
	GPIO16	7	11			
	GPIO27	8	12			
	GPIO18	—	13			
	GPIO19	—	14			
	GPIO20	9	15			
	GPIO21	10	16			
	GPIO22	—	18			
	GPIO23	—	19			
	GPIO24	12	20			
	GPIO25	—	21			
	GPIO0	—	22			
	GPIO1	—	23			
	GPIO2	—	24			
	GPIO3	14	26			
	GPIO4	15	27			
	GPIO5	—	29			
	GPIO6	19	32			
	GPIO7	—	33			

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Table 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descripitions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
I^2C	I2C0_SCL	8	12	I/O	I/O	I^2C clock data
		12	20			
		—	21			
		19	32			
	I2C0_SDA	3	2	I/O	I/O	I^2C data
		5	6			
		7	11			
		—	22			
LRF Digital Output	LRFD3	—	3	I/O	O	LRF digital ouptut 3
	LRFD0	4	5			LRF digital output 0
		14	26			
	LRFD5	—	9			LRF digital output 5
	LRFD1	10	16			LRF digital output 1
		15	27			
	LRFD7	—	23			LRF digital output 7
	LRFD6	—	29			LRF digital output 6
	LRFD2	19	32			LRF digital output 2
	LRFD4	—	33			LRF digital output 4
Power	VDDR	2	1	—	—	Internal supply
		20	34			
	VDDS	—	8	—	—	1.71-V to 3.8V DIO supply
		11	17			
		18	31			
		24	38			
	VDDD	16	28	—	—	For decoupling of internal 1.28-V regulated core-supply.
	DCDC	17	30	—	—	Switching node of internal DC/DC converter
Reset	RSTN	13	25	—	—	Global master device reset (active low)
RF	ANT	1	39			WLAN analog RF 802.11 b/g bands
RF Gound	RFGND	—	40	—	—	RF Ground reference

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Table 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descripitions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
SPI	SPI0SCLK	3	2	I/O	I/O	General SPI clock
		8	12			
		—	13			
		12	20			
	SPI0MISO	4	5	I/O	I/O	General SPI MISO
		5	6			
		6	7			
		9	15			
		10	16			
		—	21			
	SPI0CSN	4	5	I/O	I/O	General SPI chip select
		—	22			
		19	32			
	SPI0MOSI	5	6	I/O	I/O	General SPI MOSI
		6	7			
		7	11			
		—	14			
		15	27			
SWD	SWDIO	7	11	I/O	I/O	JTAG/SWD TCK. Reset default pinout.
	SWDCK	8	12	I/O	I	JTAG/SWD TMS. Reset default pinout.
Timers - Capture/ Compare	T0C0	4	5	I/O	O	Capture/compare Output-0 from Timer-0
	T0C1	10	16			Capture/compare Output-1 from Timer-0
	T0C2	8	12			Capture/compare Output-2 from Timer-0
		15	27			
	T1C0	9	15	I/O	O	Capture/compare Output-0 from Timer-1
		12	20			
	T1C1	5	6			Capture/compare Output-1 from Timer-1
	T1C2	7	11			Capture/compare Output-2 from Timer-1
		14	26			
		19	32			
	T2C0	—	18	I/O	O	Capture/compare Output-0 from Timer-2
	T2C1	—	19			Capture/compare Output-1 from Timer-2
	T2C2	—	29			Capture/compare Output-2 from Timer-2
	T3C0	—	3	I/O	O	Capture/compare Output-0 from Timer-3
		—	13			
		12	20			
	T3C1	—	14			Capture/compare Output-1 from Timer-3
		—	23			
		14	26			
		—	33			
	T3C2	—	9			Capture/compare Output-2 from Timer-3
		—	22			

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Table 7-6. RKP (QFN40) and RGE (QFN24) Peripheral Signal Descripitions (continued)

FUNCTION	SIGNAL NAME	Pin No.		PIN TYPE	SIGNAL DIRECTION	DESCRIPTION
		QFN24	QFN40			
Timers - Complimentary Capture/ Compare	T0C0N	3	2	I/O	O	Complimentary compare/PWM Output-0 from Timer-0
		6	7			
	T0C1N	14	26			Complimentary compare/PWM Output-1 from Timer-0
	T0C2N	15	27			Complimentary compare/PWM Output-2 from Timer-0
	T1C0N	3	2	I/O	O	Complimentary compare/PWM Output-0 from Timer-1
		7	11			
	T1C1N	8	12			Complimentary compare/PWM Output-1 from Timer-1
		10	16			
	T1C2N	4	5			Complimentary compare/PWM Output-2 from Timer-1
		—	9			
	T2C0N	—	10	I/O	O	Complimentary compare/PWM Output-0 from Timer-2
	T2C1N	—	24			Complimentary compare/PWM Output-1 from Timer-2
	T2C2N	—	21			Complimentary compare/PWM Output-2 from Timer-2
	T3C0N	—	3	I/O	O	Complimentary compare/PWM Output-0 from Timer-3
	T3C1N	—	18			Complimentary compare/PWM Output-1 from Timer-3
	T3C2N	—	19			Complimentary compare/PWM Output-2 from Timer-3
Timers - Fault input	T1F	6	7	I/O	I	Fault input for Timer-1
		—	9			
		—	23			
Timers - Prescaler Event	T2PE	—	4	I/O	O	Prescaler event ouput from Timer-2
		—	14			
	T0PE	12	20	I/O	O	Prescaler eveny ouput from Timer-0
		—	24			
UART	UART0TXD	6	7	I/O	O	UART0 TX data
		8	12			
		—	13			
		9	15			
		15	27			
		19	32			
	UART0RXD	5	6	I/O	I	UART0 RX data
		—	10			
		7	11			
		9	15			
		—	18			
	UART0CTS	10	16	I/O	I	UART0 clear-to-send input (active low)
		—	24			
	UART0RTS	3	2	I/O	O	UART0 request-to-send (active low)
		—	23			

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
VDDS	Supply voltage	–0.3	4.1	V
	Voltage on any digital pin(3)	–0.3	VDDS + 0.3, max 4.1	V
	Voltage on crystal oscillator pins X48P and X48N	–0.3	VDDR + 0.3, max 2.25	V
V_{in_adc}	Voltage on ADC input	0	VDDS	V
	Input level, RF pins		5	dBm
T_{stg}	Storage temperature	–40	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to ground, unless otherwise noted.
(3) Including analog capable DIOs.

8.2 ESD Ratings

				VALUE	UNIT
V_{ESD}	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	All pins	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Operating ambient temperature(1) (3)	–40	125	°C
Operating junction temperature(1) (3)	–40	125	°C
Operating supply voltage (VDDS)	1.71	3.8	V
Rising supply voltage slew rate	0	100	mV/µs
Falling supply voltage slew rate(2)	0	20	mV/µs

(1) Operation at or near maximum operating temperature for extended durations will result in a reduction in lifetime.
(2) For small coin-cell batteries, with high worst-case end-of-life equivalent source resistance, a 10-µF VDDS input capacitor must be used to ensure compliance with this slew rate.
(3) For thermal resistance characteristics refer to Section 8.3.

8.4 DCDC

When measured on the CC2340R reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for DCDC operation	(1)	2.2	3.0	3.8	V
Inductor at VDDR pin	Allowable component with typical value on PCB		10		µH
Load capacitor at VDDR pin	Required range to support		10		µF
Average recharge current	Programmable range = min value; VDDS = 3.0V (2) (3)		9		mA
Average recharge current	Programmable range = min value; VDDS = 2.2V (2) (3)		TBA		mA
Average recharge current	Programmable range = max value; VDDS = 3.0V (2) (3)		TBA		mA

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When measured on the CC2340R reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Average recharge current	Programmable range = max value; VDDS = 2.2V (2) (3)		TBA		mA

(1) When the supply voltage drops below the DCDC operation min voltage, the device smoothly transitions to use GLDO regulator on-chip.
(2) Average recharge current drawn by the device for 20-40us typical recharge times. Considers 10uH inductor (with 20% tolerance) and 10uF capacitor (with 20% tolerance) at VDDR pin.
(3) Recharge current is supplied by the battery supply and the decoupling caps at the supply. Current drawn by the battery alone would be determined by the battery series resistance (at given voltage and temperature) and decoupling capacitor at the supply pin that filter the recharge peaks and additionally the battery supply voltage which determines that DCDC dutycycle. Refer to the app note “CC23xx regulator operation and configuration” for additional details.

8.5 GLDO

When measured on the CC2340R reference design with T_c = 25 °C, V_{DDS} = 3.0 V with DC/DC enabled unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS supply voltage for GLDO operation	To meet performance specifications	1.71	3.0	3.8	V
Load capacitor at VDDR pin	Required range to support	TBA	10	TBA	µF

8.6 PMU_POR_BOD

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDDS_BOD					
Untrimmed brownout rising threshold	Before initial boot (1)	1.53	1.62	1.71	V
Trimmed brownout rising threshold	(1)	1.659	1.68	1.71	V
Trimmed brownout falling threshold	(1)	1.63	1.66	1.69	V
VDD_BOD					
POR					
VDDS rising rate		0		100	mV/µs
VDDS falling rate		0		20	mV/µs
power-on reset power-up level		1.35	1.5	1.66	V
power-on reset power-down level		1.30	1.45	1.59	V
power-on reset power-down level	Between 125℃ and 150℃			1.71	V

(1) Brown-out Detector is trimmed at initial boot, value is kept until device is reset by a POR reset or the RESET_N pin

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8.7 Power Consumption - Power Modes

When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V unless otherwise noted. DCDC disabled, GLDO enabled.

PARAMETER		TEST CONDITIONS	TYP	UNIT
Core Current Consumption with DCDC				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	2.6	mA
I_{core}	Active	MCU running CoreMark from SRAM at 48 MHz	1.6	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	530	µA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	564	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	864	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	981	µA
I_{core}	Standby	RTC running, 36kB RAM retention. LFOSC, DCDC recharge current setting (ipeak = 7)	0.7	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT DCDC recharge current setting: ipeak = 7	0.77	uA
Core Current consumption with GLDO				
I_{core}	Active	MCU running CoreMark from Flash at 48 MHz	4.4	mA
I_{core}	Active	MCU running CoreMark from SRAM at 48 MHz	TBA	mA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA disabled	TBA	µA
I_{core}	Idle	Supply Systems and RAM powered, flash disabled, DMA enabled	TBA	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA disabled	TBA	µA
I_{core}	Idle	Supply Systems and RAM powered, flash enabled, DMA enabled	TBA	µA
I_{core}	Standby	RTC running, 36kB RAM retention. LFOSC, max GLDO recharge current setting	1	µA
I_{core}	Standby	RTC running, 36kB RAM retention LFXT max GLDO recharge current setting	1.15	uA
Reset, Shutdown Current Consumption				
I_{core}	Reset	Reset. RESET_N pin asserted or VDDS below power-on-reset threshold	150	nA
I_{core}	Shutdown	Shutdown. No clocks running, no retention, IO wakeup enabled	150	nA
I_{VDDS}	Startup	Inrush current on cold boot into the device for GLDO charging (4)	10	mA
I_{VDDS}	Startup	Inrush current into the device upon wakeup from reset/shutdown/thermal shutdown for GLDO charging, 4.7mA GLDO current setting (6) (5)	5	mA
I_{VDDS}	Startup	Inrush current into the device upon wakeup from reset/shutdown/thermal shutdown for GLDO charging, max GLDO current setting (6) (5)	82	mA
Peripheral Current Consumption				
I_{peri}	RF	Delta current, clock enabled, RF subsystem idle	TBA	µA
I_{peri}	Timers	Delta current with clock enabled, module is idle, one LGPT timer	81.0	µA
I_{peri}	WDT	Delta current with WDT enabled and operational in standby mode, 32kHz clock	TBA	nA
I_{peri}	I2C	Delta current with clock enabled, module is idle (2)	10.1	µA
I_{peri}	SPI	Delta current with clock enabled, module is idle (3)	82.9	µA
I_{peri}	UART	Delta current with clock enabled, module is idle(1)	167.5	µA
I_{peri}	uDMA	Delta current with clock enabled, 1 channel, burst mode, moving 16B data from SPI buffer to device RAM	TBA	µA/MHz
I_{peri}	CRYPTO (AES)	Delta current with clock enabled, module is idle(3)	25.6	µA

(1) Only one UART running
(2) Only one I2C running
(3) Only one SPI running
(4) Inrush current during cold boot for charging VDDS capacitor is not part of this specification and is dependent on the battery series resistance and decoupling capacitor at the supply VDDS pin.
(5) 3V domain register bit setting for GLDO charge current setting is configured by application SW.
(6) The peak current is drawn for short time in case the device has not been in reset/shutdown/thermal shutdown for sufficient time to discharge the VDDR capacitor.

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8.8 Nonvolatile (Flash) Memory Characteristics

Over operating free-air temperature range and V_{DDS} = 3.0 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Flash sector size			2		KB
Supported flash erase cycles before failure, full bank(1) (5)		30			k Cycles
Supported flash erase cycles before failure, single sector(2)		60			k Cycles
Maximum number of write operations per row before sector erase(3)				83	Write Operations
Flash retention	105 °C	11.4			Years
Flash retention	125 °C	TBA			Years
Flash sector erase current	Average delta current		10.7		mA
Flash sector erase time(4)	0 erase cycles		10		ms
Flash write current	Average delta current, 4 bytes at a time		6.2		mA
Flash write time(4)	4 bytes at a time		21.6		µs

(1) A full bank erase is counted as a single erase cycle on each sector
(2) Up to 16 customer-designated sectors can be individually erased an additional 30k times beyond the baseline bank limitation of 30k cycles
(3) Each wordline is 2048 bits (or 256 bytes) wide. This limitation corresponds to sequential memory writes of 4 (3.1) bytes minimum per write over a whole wordline. If additional writes to the same wordline are required, a sector erase is required once the maximum number of write operations per row is reached.
(4) This number is dependent on Flash aging and increases over time and erase cycles
(5) Aborting flash during erase or program modes is not a safe operation.

8.9 Thermal Resistance Characteristics

THERMAL METRIC	THERMAL METRIC	PACKAGE		UNIT
		RKP (VQFN)	RGE (VQFN)	
		40 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	TBA	TBA	°C/W (1)
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	TBA	TBA	°C/W (1)
$R_{\theta JB}$	Junction-to-board thermal resistance	TBA	TBA	°C/W (1)
ψ_{JT}	Junction-to-top characterization parameter	TBA	TBA	°C/W (1)
ψ_{JB}	Junction-to-board characterization parameter	TBA	TBA	°C/W (1)
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	TBA	TBA	°C/W (1)

(1) °C/W = degrees Celsius per watt.

8.10 Thermal Shutdown

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OP}	Operating supply voltage		1.71		3.8	V
T_{jun}	Operating junction temperature		96		150	°C
T_{rstrel}	Reset release temperature		101.8		114	°C
I_{core_TSD}	Current consumption in thermal shutdown mode (up to 150C)				100	µA

8.11 RF Frequency Bands

Over operating free-air temperature range (unless otherwise noted).

PARAMETER	MIN	TYP	MAX	UNIT
Frequency bands	2360		2500	MHz

8.12 Bluetooth Low Energy - Receive (RX)

When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
125 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–102		dBm
Receiver saturation	BER = 10^{-3}		>5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–320 / 240)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–125 / 125)		ppm
Co-channel rejection(1)	Wanted signal at –79 dBm, modulated interferer in channel, BER = 10^{-3}		–1.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4.5(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 39(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 44(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		44 / 46(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –79 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		48 / 44(2)		dB
Selectivity, ±7 MHz	Wanted signal at –79 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		51 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –79 dBm, modulated interferer at image frequency, BER = 10^{-3}		39		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –79 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4.5 / 44 (2)		dB
500 kbps (LE Coded)					
Receiver sensitivity	BER = 10^{-3}		–99		dBm
Receiver saturation	BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–300 / 300)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–450 / 450)		ppm
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (255-byte packets)		> (–175 / 175)		ppm
Co-channel rejection(1)	Wanted signal at –72 dBm, modulated interferer in channel, BER = 10^{-3}		–3.5		dB
Selectivity, ±1 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±2 MHz, BER = 10^{-3}		44 / 37(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		46 / 46(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		45 / 47(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –72 dBm, modulated interferer at ≥ ±6 MHz, BER = 10^{-3}		46 / 45(2)		dB
Selectivity, ±7 MHz	Wanted signal at –72 dBm, modulated interferer at ≥ ±7 MHz, BER = 10^{-3}		49 / 45(2)		dB
Selectivity, Image frequency(1)	Wanted signal at –72 dBm, modulated interferer at image frequency, BER = 10^{-3}		37		dB
Selectivity, Image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –72 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 46(2)		dB

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When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
1 Mbps (LE 1M)					
Receiver sensitivity	BER = 10^{-3}		–96		dBm
Receiver saturation	BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–350 / 350)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–750 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel, BER = 10^{-3}		–6		dB
Selectivity, ±1 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±1 MHz, BER = 10^{-3}		7 / 4(2)		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz,BER = 10^{-3}		40 / 33(2)		dB
Selectivity, ±3 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±3 MHz, BER = 10^{-3}		36 / 41(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 45(2)		dB
Selectivity, ±5 MHz or more(1)	Wanted signal at –67 dBm, modulated interferer at ≥ ±5 MHz, BER = 10^{-3}		40		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		33		dB
Selectivity, image frequency ±1 MHz(1)	Note that Image frequency + 1 MHz is the Co- channel –1 MHz. Wanted signal at –67 dBm, modulated interferer at ±1 MHz from image frequency, BER = 10^{-3}		4 / 41(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–10		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–18		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–12		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–2		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2405 and 2408 MHz respectively, at the given power level		–42		dBm
Spurious emissions, 30 to 1000 MHz(4)	Measurement in a 50-Ω single-ended load.		< –59		dBm
Spurious emissions, 1 to 12.75 GHz(4)	Measurement in a 50-Ω single-ended load.		< –47		dBm
RSSI dynamic range			70		dB
RSSI accuracy			±4		dB
RSSI resolution			1		dB
2 Mbps (LE 2M)					
Receiver sensitivity	Measured at SMA connector, BER = 10^{-3}		–91		dBm
Receiver saturation	Measured at SMA connector, BER = 10^{-3}		> 5		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> (–500 / 500)		kHz
Data rate error tolerance	Difference between incoming data rate and the internally generated data rate (37-byte packets)		> (–700 / 750)		ppm
Co-channel rejection(1)	Wanted signal at –67 dBm, modulated interferer in channel,BER = 10^{-3}		–7		dB
Selectivity, ±2 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±2 MHz, Image frequency is at –2 MHz, BER = 10^{-3}		8 / 4(2)		dB
Selectivity, ±4 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±4 MHz, BER = 10^{-3}		36 / 36(2)		dB
Selectivity, ±6 MHz(1)	Wanted signal at –67 dBm, modulated interferer at ±6 MHz, BER = 10^{-3}		37 / 36(2)		dB
Selectivity, image frequency(1)	Wanted signal at –67 dBm, modulated interferer at image frequency, BER = 10^{-3}		4		dB

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When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Selectivity, image frequency ±2 MHz(1)	Note that Image frequency + 2 MHz is the Co-channel. Wanted signal at –67 dBm, modulated interferer at ±2 MHz from image frequency, BER = 10^{-3}		–7 / 36(2)		dB
Out-of-band blocking(3)	30 MHz to 2000 MHz		–16		dBm
Out-of-band blocking	2003 MHz to 2399 MHz		–21		dBm
Out-of-band blocking	2484 MHz to 2997 MHz		–15		dBm
Out-of-band blocking	3000 MHz to 12.75 GHz		–12		dBm
Intermodulation	Wanted signal at 2402 MHz, –64 dBm. Two interferers at 2408 and 2414 MHz respectively, at the given power level		–38		dBm

(1) Numbers given as I/C dB
(2) X / Y, where X is +N MHz and Y is –N MHz
(3) Excluding one exception at F_{wanted} / 2, per Bluetooth Specification
(4) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan)

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8.13 Bluetooth Low Energy - Transmit (TX)

When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Delivered to a single-ended 50-Ω load through integrated balun		8		dBm
Output power programmable range	Delivered to a single-ended 50-Ω load through integrated balun		29		dB

8.14 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - RX

Measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Receiver sensitivity	PER = 1%		–98		dBm
Receiver saturation	PER = 1%		> 5		dBm
Adjacent channel rejection	Wanted signal at –82 dBm, modulated interferer at ±5 MHz, PER = 1%		36		dB
Alternate channel rejection	Wanted signal at –82 dBm, modulated interferer at ±10 MHz, PER = 1%		57		dB
Channel rejection, ±15 MHz or more	Wanted signal at –82 dBm, undesired signal is IEEE 802.15.4 modulated channel, stepped through all channels 2405 to 2480 MHz, PER = 1%		59		dB
Blocking and desensitization, 5 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		57		dB
Blocking and desensitization, 10 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 20 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, 50 MHz from upper band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		66		dB
Blocking and desensitization, –5 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –10 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		60		dB
Blocking and desensitization, –20 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		63		dB
Blocking and desensitization, –50 MHz from lower band edge	Wanted signal at –97 dBm (3 dB above the sensitivity level), CW jammer, PER = 1%		65		dB
Spurious emissions, 30 MHz to 1000 MHz	Measurement in a 50-Ω single-ended load(1)		–66		dBm
Spurious emissions, 1 GHz to 12.75 GHz	Measurement in a 50-Ω single-ended load(1)		–53		dBm
Frequency error tolerance	Difference between the incoming carrier frequency and the internally generated carrier frequency		> 350		ppm
Symbol rate error tolerance	Difference between incoming symbol rate and the internally generated symbol rate		> 1000		ppm
RSSI dynamic range			95		dB
RSSI accuracy			±4		dB

(1) Suitable for systems targeting compliance with EN 300 328, EN 300 440 class 2 (Europe), FCC CFR47, Part 15 (US) and ARIB STD-T-66 (Japan)

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8.15 Zigbee and Thread - IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps) - TX

Measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
General Parameters					
Max output power	Delivered to a single-ended 50-Ω load through integrated balun		8		dBm
Output power programmable range	Delivered to a single-ended 50-Ω load through integrated balun		29		dB
IEEE 802.15.4-2006 2.4 GHz (OQPSK DSSS1:8, 250 kbps)					
Error vector magnitude	+8 dBm setting		TBA		%

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8.16 Proprietary Radio Modes

Measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF}= 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
HID fast mode 2 Mbps					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
Radio Command to Transmit time	Time between triggering radio Tx command to when the radio transmits first preamble bit over air (frequency channel configuration, not included) (1)		40		us
Radio Command to Receive time	Time between triggering radio Rx command to when the radio receives the first preamble bit (frequency channel configuration, not included) (1)		40		us
Radio turnaround time	Time period between radio Tx to Rx or Rx to Tx turnaround		40		us
2 Mbps GFSK (HID), 320 kHz deviation					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
1 Mbps GFSK, 160 kHz deviation					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
250 kbps GFSK, 160 kHz deviation					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
100 kbps GFSK, 50 kHz deviation					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
250 kbps GFSK, 125 kHz deviation					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
500 kbps MSK					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm
250 kbps MSK (CC2510)					
Receiver sensitivity	PER = TBD%, Payload TBD		TBD		dBm

(1) The radio is preinitialized, before Tx/Rx command is executed. The time period from Tx/Rx command execution to radio ready to transmit/receive does not consider changing the channel frequency.

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8.17 2.4 GHz RX/TX CW

When measured on the LP-EM-CC2340R5 reference design with T_c = 25 °C, V_{DDS} = 3.0 V, f_{RF} = 2440 MHz with DC/DC enabled unless otherwise noted. All measurements are performed at the antenna input with a combined RX and TX path. All measurements are performed conducted.

PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
Spurious emissions and harmonics						
Spurious emissions[1]	f < 1 GHz, outside restricted bands	+8 dBm setting		< –36		dBm
	f < 1 GHz, restricted bands ETSI			< –54		dBm
	f < 1 GHz, restricted bands FCC			< –55		dBm
	f > 1 GHz, including harmonics			< –42		dBm
Harmonics [1]	Second harmonic			< –42		dBm
	Third harmonic			< –42		dBm

(1) Suitable for systems targeting compliance with worldwide radio-frequency regulations ETSI EN 300 328 and EN 300 440 Class 2 (Europe), FCC CFR47 Part 15 (US), and ARIB STD-T66 (Japan).

8.18 Timing and Switching Characteristics

8.18.1 Reset Timing

PARAMETER	MIN	TYP	MAX	UNIT
RESET_N low duration	1			µs

8.18.2 Wakeup Timing

Measured over operating free-air temperature with V_{DDS} = 3.0 V (unless otherwise noted). The times listed here do not include any software overhead (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
MCU, Reset/Shutdown to Active[1]		GLDO default charge current setting, VDDR capacitor fully charged [2]		550		µs
MCU, Reset/ Shutdown to Active[1]	MCU, Reset/Shutdown/Thermal Shutdown to Active[1]	GLDO default charge current setting, VDDR capacitor fully discharged [3]		2000		µs
MCU, Reset/ Shutdown to Active[1]	MCU, Reset/Shutdown/Thermal Shutdown to Active[1]	GLDO charge current setting 4.7mA average current), VDDR capacitor fully discharged [3]		3500		µs
MCU, Reset/ Shutdown to Active[1]	MCU, Reset/Shutdown/Thermal Shutdown to Active[1]	GLDO charge current setting(max average current), VDDR capacitor fully discharged [3]		250		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash)	DCDC ON, max recharge current configuration		50		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash)	DCDC ON, min recharge current configuration		80		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash)	GLDO ON, max recharge current configuration		80		µs
MCU, Standby to Active	MCU, Standby to Active (ready to execute code from flash)	GLDO ON, min recharge current configuration		200		µs
MCU, Active to Standby				50		µs
MCU, Idle to Active		Flash enabled in idle mode		100		ns
MCU, Idle to Active	MCU, Idle to Active	Flash disabled in idle mode		10		µs

(1) Wakeup time includes device ROM bootcode execution time. The wakeup time is dependent on remaining charge on VDDR capacitor when starting the device, and thus how long the device has been in Reset or Shutdown before starting up again.
(2) This is the best case reset/shutdown to active time (including ROM bootcode operation), for the specified GLDO charge current setting considering the VDDR capacitor is fully charged and is not discharged during the reset and shutdown events; that is, when the device is in reset / shutdown modes for only a very short period of time

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(3) Considers wakeup from device cold boot (from power off state) or reset/shutdown/thermal shutdown state after the device has been in this state for duration of time where-in the VDDR capacitor is fully discharge (typically 10-15minutes)

8.18.3 Clock Specifications

8.18.3.1 48 MHz Crystal Oscillator (HFXT)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	PARAMETER	MIN	TYP	MAX	UNIT
	Crystal frequency		48		MHz
ESR	Equivalent series resistance 6 pF < C_L ≤ 9 pF		20	60	Ω
ESR	Equivalent series resistance 5 pF < C_L ≤ 6 pF			80	Ω
L_M	Motional inductance, relates to the load capacitance that is used for the crystal (C_L in Farads)(4)		< 3 × 10^{-25} / C_L ^{2}		H
C_L	Crystal load capacitance(3)	3	7(2)	9	pF
Start-up time(1)	Until clock is qualified		200		µs

(1) Start-up time using the TI-provided power driver. Start-up time may increase if driver is not used.
(2) On-chip default connected capacitance including reference design parasitic capacitance. Connected internal capacitance is changed through software in the Customer Configuration section (CCFG).
(3) Adjustable load capacitance is integrated into the device. External load capacitors are required for systems targeting compliance with certain regulations.
(4) The crystal manufacturer's specification must satisfy this requirement for proper operation.

8.18.3.2 48 MHz RC Oscillator (HFOSC)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

	MIN	TYP	MAX	UNIT
Frequency		48		MHz
Uncalibrated frequency accuracy		±1		%
Calibrated frequency accuracy(1)		±0.25		%
Start-up time		5		µs

(1) Accuracy relative to the calibration source (HFXT)

8.18.3.3 32 kHz Crystal Oscillator (LFXT)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Crystal frequency			32.768		kHz
Supported crystal load capacitance		6		12	pF
ESR			30	100	kΩ

8.18.3.4 32 kHz RC Oscillator (LFOSC)

Measured on a Texas Instruments reference design with T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

		MIN	TYP	MAX	UNIT
Calibrated frequency			32.768 (1)		kHz
Temperature coefficient.	Temperature coefficient.		±50		ppm/°C

(1) When using LFOSC as source for the low frequency system clock (LFCLK), the accuracy of the LFCLK-derived Real Time Clock (RTC) can be improved by measuring LFOSC relative to HFXT and compensating for the RTC tick speed. This functionality is available through the TI-provided Power driver.

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8.19 Peripheral Characteristics

8.19.1 UART Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	MIN	TYP	MAX	UNIT
UART rate			3	MBaud

8.19.2 SPI Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
fSCLK 1/tsclk	SPI clock frequency	Primary Mode 1.71 < VDDS < 3.8			12	MHz
		Secondary Mode 2.7 < VDDS < 3.8			8	
		Secondary Mode VDDS < 2.7			7	
DC_{SCK}	SCK Duty Cycle		45	50	55	%

8.19.3 SPI Primary Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tCS.LEAD	CS lead-time, CS active to clock		1			SPIclk
tCS.LAG	CS lag time, Last clock to CS inactive		1			SPIclk
tCS.ACC	CS access time, CS active to MOSI data out				1	SPIclk
tCS.DIS	CS disable time, CS inactive to MOSI high inpedance				1	SPIclk
tSU.MI	MISO input data setup time	VDDS = 3.3V	12.5			ns
tSU.MI	MISO input data setup time	VDDS = 1.8V	23.5			ns
tHD.MI	MISO input data hold time		0			ns
tVALID.MO	MOSI output data valid time(2)	UCLK edge to MOSI valid,CL = 20 pF (4)			13	ns
tHD.MO	MOSI output data hold time (3)	CL = 20 pF	0			ns

8.19.4 SPI Secondary Mode

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tCS.LEAD	CS lead-time, CS active to clock		0.5			ns
tCS.LAG	CS lag time, Last clock to CS inactive		0.5			ns
tCS.ACC	CS access time, CS active to MISO data out	VDDS = 3.3V			56	ns
tCS.ACC	CS access time, CS active to MISO data out	VDDS = 1.8V			70	ns
tCS.DIS	CS disable time, CS inactive to MISO high inpedance	VDDS = 3.3V			56	ns
tCS.DIS	CS disable time, CS inactive to MISO high inpedance	VDDS = 1.8V			70	ns
tSU.SI	MOSI input data setup time		30			ns
tHD.SI	MOSI input data hold time		0			ns

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
tVALID.SO	MISO output data valid time	UCLK edge to MISO valid,CL = 20 pF, 3.3V (4)			50	ns
tVALID.SO	MISO output data valid time	UCLK edge to MISO valid,CL = 20 pF, 1.8V (4)			65	ns
tHD.SO	MISO output data hold time	CL = 20 pF	0			ns

8.19.5 I2C

over operating free-air temperature range (unless otherwise noted)

PARAMETERS		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{SCL}	SCL clock frequency		0		400	kHz
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} = 100kHz	4.0			us
$t_{HD,STA}$	Hold time (repeated) START	f_{SCL} > 100kHz	0.6			us
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} = 100kHz	4.7			us
$t_{SU,STA}$	Setup time for a repeated START	f_{SCL} > 100kHz	0.6			us
$t_{HD,DAT}$	Data hold time		0			us
$t_{SU,DAT}$	Data setup time		100			us
$t_{SU,STO}$	Setup time for STOP	f_{SCL} = 100kHz	4.0			us
$t_{SU,STO}$	Setup time for STOP	f_{SCL} > 100kHz	0.6			us
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} = 100kHz	4.7			us
t_{BUF}	Bus free time between STOP and START conditions	f_{SCL} > 100kHz	1.3			us
t_{SP}	Pulse duration of spikes supressed by input deglitch filter		50		tba	ns

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8.19.6 GPIO

8.19.6.1 GPIO DC Characteristics

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_A = 25 °C, V_{DDS} = 1.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		73		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		19		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.08		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		0.73		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.35		V
T_A = 25 °C, V_{DDS} = 3.0 V					
GPIO VOH at 10 mA load	high-drive GPIOs only, max drive setting		2.85		V
GPIO VOL at 10 mA load	high-drive GPIOs only, max drive setting		0.15		V
GPIO VOH at 2 mA load	standard drive GPIOs		2.9		V
GPIO VOL at 2 mA load	standard drive GPIOs		0.1		V
T_A = 25 °C, V_{DDS} = 3.8 V					
GPIO pullup current	Input mode, pullup enabled, Vpad = 0 V		282		µA
GPIO pulldown current	Input mode, pulldown enabled, Vpad = VDDS		110		µA
GPIO low-to-high input transition, with hysteresis	IH = 1, transition voltage for input read as 0 → 1		1.97		V
GPIO high-to-low input transition, with hysteresis	IH = 1, transition voltage for input read as 1 → 0		1.55		V
GPIO input hysteresis	IH = 1, difference between 0 → 1 and 1 → 0 points		0.42		V
T_A = 25 °C					
VIH	Lowest GPIO input voltage reliably interpreted as a *High*	0.8*V_{DDS}			V
VIL	Highest GPIO input voltage reliably interpreted as a *Low*			0.2*V_{DDS}	V

8.19.7 ADC

Analog-to-Digital Converter (ADC) Characteristics

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC Power Supply and Input Range Conditions						
$V_{(Ax)}$	Analog input voltage range	All ADC analog input pins Ax	0		VDDS	V
$I_{(ADC)}$ single-ended mode	Operating supply current into VDDS terminal	RES = 0x0 (12Bit mode), Fs = 1.2MSPS, Internal reference OFF (ADCREF_EN = 0), VeREF+ = VDDS		300	TBD	µA
		RES = 0x0 (12Bit mode), Fs = 266ksps, Internal reference ON (ADCREF_EN = 0), ADCREF = 2.5V		250	TBD	
$C_{I\ GPIO}$	Input capacitance into a single terminal			5	7	pF
$R_{I\ GPIO}$	Input MUX ON-resistance			0.5	1	kΩ
ADC Switching Characteristics						
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x0 (12Bits), VDDS = 1.71V to VDDSmax			267	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x1 (10Bits), VDDS = 1.71V to VDDSmax			308	ksps
F_S ADC REF	ADC sampling frequency when using the internal ADC reference voltage	ADCREF_EN = 1, RES = 0x2 (8Bits), VDDS = 1.71V to VDDSmax			400	ksps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x0 (12Bits), VDDS = 1.71V to VDDSmax			1.2	Msps

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x1 (10Bits), VDDS = 1.71V to VDDSmax			1.33	Msps
F_S EXTREF	ADC sampling frequency when using the external ADC reference voltage	ADCREF_EN = 0, VeREF+ = VDDS, RES = 0x2 (8Bits), VDDS = 1.71V to VDDSmax			1.6	Msps
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x0 (12Bits)		14		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x1 (10Bits)		12		cycles
$N_{CONVERT}$	Clock cycles for conversion	RES = 0x2 (8Bits)		9		cycles
T_{ADCON}	ADC turn-on settling time	Assumes the reference is active			5	us
t_{Sample}	Sampling time	RES = 0x0 (12-bit), R_S = 25 Ω, C_{pext} = 10 pF. +/- 0.5 LSB settling	250			ns
$t_{VSUPPLY/3(sample)}$	Sample time required when Vsupply/3 channel is selected		20			µs
ADC Linearity Parameters						
E_I	Integral linearity error (INL) for single-ended inputs	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8	-2.0		+2.0	LSB
E_D	Differential linearity error (DNL)	12-bit Mode, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8	>-1.0		+1.0	LSB
E_O	Offset error	External reference, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8	-1	+/- 0.2	1	mV
E_O	Offset error	Internal reference, V_{R+} = ADCREF = 2.5V	-1	+/- 0.2	1	mV
E_G	Gain error	External Reference, V_{R+} = VeREF+ = VDDS , VDD= 1.71-->3.8	-3	+/- 2	3	LSB
E_G	Gain error	Internal reference, V_{R+} = ADCREF = 2.5V	-120	+/- 40	120	LSB
E_T	Total unadjusted error	External reference, V_{R+} = VeREF+ = VDDS, VDDS=1.71-->3.8		TBA	TBA	LSB
E_T	Total unadjusted error	Internal reference, V_{R+} = ADCREF = 2.5V		TBA	TBA	LSB
ADC Dynamic Parameters						
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x2 (8-bit)		TBA		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x1 (10-bit)		TBA		bit
ENOB	Effective number of bits	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)		11.2		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x2 (8-bit)		TBA		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V} , RES = 0x1 (10-bit)		TBA		bit
ENOB	Effective number of bits	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)		TBA		bit
ENOB	Effective number of bits	VDDS reference, RES = 0x0 (12-bit)		TBA		bit
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V, RES = 0x0 (12-bit)	TBA	TBA		dB
SINAD	Signal-to-noise and distortion ratio	ADCREF_EN = 1, ADCREF_VSEL = {2.5V, 1.4V}, RES = 0x0 (12-bit)	TBA	TBA		dB
SINAD	Signal-to-noise and distortion ratio	VDDS reference, RES = 0x0 (12-bit)	TBA	TBA		dB
PSRR_DC	Power supply rejection ratio, DC	VDDS = VDDS(min) to VDDS(max) ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V		TBA		dB
PSRR_DC	Power supply rejection ratio, DC	VDDS = VDDS(min) to VDDS(max) ADCREF_EN = 1, ADCREF_VSEL = 2.5V		TBA		dB
PSRR_AC	Power supply rejection ratio, AC	ΔVDDS = 0.1 V at 1 kHz ADCREF_EN = 0, VeREF+ = VDDS =3.3V, VeREF-=0V		TBA		dB
PSRR_AC	Power supply rejection ratio, AC	ΔVDDS = 0.1 V at 1 kHz ADCREF_EN = 1, ADCREF_VSEL = 2.5V		TBA		dB

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T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.(1)
Performance numbers require use of offset and gain adjustements in software by TI-provided ADC drivers.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ADC External Reference						
EXTREF	Positive external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF+)	1.4		VDDS	V
EXTREF	Negative external reference voltage input	ADCREF_EN=0, ADC reference sourced from external reference pin (VeREF-)			0	V
I_{VeREF+} I_{VeREF-}	ADC external reference current consumption	ADCREF_EN=0, 1.4 V ≤ VeREF+≤ VDDS, VeREF- = 0 V, f_{ADCCLK} = 48 MHz,		TBA		µA
C_{VeREF+}	Capacitance at VeREF+ terminal		TBA			µF
ADC Temperature Diode, Supply Monitor						
I_{temp_diode}	Temperature diode active current consumption			20		uA
	Sensitivity	Change of voltage per degree C	-1.7	-1.3	-1	mV/C
ADC Internal Input: V_{SUPPLY} / 3 Accuracy	V_{supply} voltage divider accuracy for supply monitoring	ADC input channel: Vsupply monitor	-1		+1	%
ADC Internal Input: $I_{Vsupply / 3}$	V_{supply} voltage divider current consumption	ADC input channel Vsupply monitor. V_{supply}=VDDS=3.3V		10		uA
ADC Internal and VDDS Reference						
VDDSREF	Positive ADC reference voltage	ADC reference sourced from VDDS		VDDS		V
ADCREF	Internal ADC Reference Voltage	ADCREF_EN = 1, ADCREF_VSEL = 0, VDDS = 1.71V - VDDSmax	1.365	1.4	1.435	V
		ADCREF_EN = 1, ADCREF_VSEL = 1, VDDS = 2.7V - VDDSmax	2.4375	2.5	2.5625	
I_{ADCREF}	Operating supply current into VDDA terminal with internal reference ON	ADCREF_EN = 1, VDDA = 1.7V to VDDAmax, ADCREF_VSEL = {0,1}		80	100	µA
t_{ON}	Internal ADC Reference Voltage power on-time	ADCREF_EN = 1			10	µs

(1) Using IEEE Std 1241-2010 for terminology and test methods

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8.19.8 Comparators

Ultra-low power comparator

T_c = 25 °C, V_{DDS} = 3.0 V, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Input voltage range		0		V_{DDS}	V
	Clock frequency			32		KHz
	Voltage Divider Accuracy	Input voltage range is between VDDS/4 and VDDS*3/4				
	Voltage divider accuracy, Vin * 1/4	Reference Division bit = 0	88.4		99.2	%
	Voltage divider accuracy, Vin * 1/2	Reference Division bit = 1	94.2		99.8	%
	Voltage divider accuracy, Vin * 3/4	Reference Division bit = 3	96.2		99.9	%
	Voltage divider accuracy, Vin * 1/3	Reference Division bit = 4	92.2		99.8	%
	Voltage divider accuracy, Vin * 1/1	Reference Division bit = 7	99.7		99.9	%
DIGLDO reference	Internal reference voltage, DIGLDO	DIGLDO, output voltage, trimmed	1.21	1.28	1.34	V
	Offset	Measured at V_{DDS} / 2 (Errors seen when using two external inputs)	-30		+30	mV
	Decision time	Step from –50 mV to 50 mV		1	3	Clock Cycle
	Comparator enable time	COMP_LP disable → enable, VIN+, VIN- from pins, Overdrive ≥ 20 mV		80		us
	Current consumption	Including using VDDS/2 as internal reference at VIN- comparator terminal		300		nA

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9 Detailed Description

9.1 Overview

Section 4 shows the core modules of the CC2340R5 device.

9.2 System CPU

The CC2340R5 SimpleLink™ Wireless MCU contains an Arm® Cortex®-M0+ system CPU, which runs the application and the higher layers of radio protocol stacks. The Cortex-M0+ processor is built on a highly area and power optimized 32-bit processor core, with a 2-stage pipeline Von Neumann architecture. The processor delivers exceptional energy efficiency through a small but powerful instruction set and extensively optimized design, providing high-end processing hardware including a single-cycle multiplier. The Cortex-M0+ processor offers multiple benefits to developers including:

- Ultra-low power, energy efficient operation
- Deterministic, high-performance interrupt handling for time-critical applications
- Upward compatibility with the Cortex-M processors family

The Cortex-M0+ processor provides the excellent performance expected of a modern 32- bit architecture core, with higher code density than other 8-bit and 16-bit microcontrollers. Its features include the following:

- ARMv6-M architecture optimized for small-footprint embedded applications
- Subset of Arm Thumb/Thumb-2 mixed 16- and 32-bit instructions delivers the high performance expected of a 32-bit Arm
- Single-cycle multiply instruction
- VTOR supporting offset of the vector table base address
- Serial Wire debug with HW break-point comparators
- Ultra-low-power consumption with integrated sleep modes
- SysTick timer
- 48 MHz operation
- 0.99 DMIPS/MHz

Additionally, the CC2340Rx devices are compatible with all ARM tools and software.

9.3 Radio (RF Core)

The low-power RF Core (LRF) implements a high performance and highly flexible RF sub system containing RF and baseband circuitry in addition to a software defined modem (LRFD). LRFD provides a high-level, command-based API to the main CPU and handles all of the timing critical and low-level details of many different radio PHYs. Several signals are also available to control external circuitry such as RF switches or range extenders autonomously.

The software-defined modem is not programmable by customers but is instead loaded with pre-compiled images provided in the radio driver in the SimpleLink Software Development Kit (SDK). This mechanism allows the radio platform to be updated for support of future versions of standards with over-the-air (OTA) updates while still using the same silicon. LRFD stores the code images in the RF SRAM and does not make use of any ROM memory, thus image loading from NV memory only occurs once after boot and also, no patching is required when exiting power modes.

A Packet Traffic Arbitrator (PTA) scheme is available for the managed coexistence of BLE and a co-located 2.4-GHz radio. This is based on 802.15.2 recommendations and common industry standards. The 3-wire coexistence interface has multiple modes of operation, encompassing different use cases and number of lines used for signaling. The radio acting as a slave is able to request access to the 2.4-GHz ISM band, and the master to grant it. Information about the request priority and TX or RX operation can also be conveyed.

9.3.1 Bluetooth 5.2 Low Energy

The RF Core offers full support for Bluetooth 5.3 Low Energy, including the high-speed 2 Mb/s physical layer and the 500 Kb/s and 125 Kb/s long range PHYs (Coded PHY) through the TI provided Bluetooth 5.3 stack or through a high-level Bluetooth API.

The new high-speed mode allows data transfers up to 2 Mb/s, twice the speed of Bluetooth 4.2 and five times the speed of Bluetooth 4.0, without increasing power consumption. In addition to faster speeds, this mode offers significant improvements for energy efficiency and wireless coexistence with reduced radio communication time.

Bluetooth 5.3 also enables unparalleled flexibility for adjustment of speed and range based on application needs, which capitalizes on the high-speed or long-range modes respectively. Data transfers are now possible at 2 Mb/s, enabling development of applications using voice, audio, imaging, and data logging that were not previously an option using Bluetooth low energy. The CC2340R5 device also supports the Bluetooth 5.3 connected and connectionless Angle of Arrival (AoA) TX feature, which enables asset tracking and indoor positioning systems. With high-speed mode, existing applications deliver faster responses, richer engagement, and longer battery life. Bluetooth 5.3 enables fast, reliable firmware updates.

9.3.2 802.15.4 (Thread and Zigbee)

Through a dedicated IEEE radio API, the RF sub-system supports the 2.4-GHz IEEE 802.15.4-2011 physical layer (2 Mchips per second Offset-QPSK with DSSS 1:8), used in Thread and Zigbee protocols. TI also provides royalty-free protocol stacks for Thread and Zigbee as part of the SimpleLink SDK, enabling a robust end-to-end solution.

9.4 Memory

The up to 512-KB nonvolatile (Flash) memory provides storage for code and data. The flash memory is in-system programmable and erasable. A special flash memory sector must contain a Customer Configuration section (CCFG) that is used by boot ROM and TI provided drivers to configure the device. This configuration is done through the ccfg.c source file that is included in all TI provided examples.

The ultra-low leakage system static 36-KB RAM (SRAM) can be used for both storage of data and execution of code. Retention of SRAM contents in Standby power mode is enabled by default and included in Standby mode power consumption numbers. System SRAM is always initialized to zeroes upon code execution during boot.

The ROM includes device bootcode firmware handling initial device trimming operations, security configurations and device lifecycle management. The ROM also contains a serial (SPI and UART) bootloader that can be used for initial programming of the device.

9.5 Cryptography

The CC2340R5 device comes with AES-128 cryptography hardware accelerator, thereby, reducing code footprint and execution time for cryptographic operations. It also has the benefit of being lower power and improves availability and responsiveness of the system because the cryptography operations run in a background hardware thread. The AES hardware accelerators supports the following block cipher modes and message authentication codes:

- AES ECB encrypt
- AES CBC encrypt
- AES CTR encrypt/decrypt
- AES CBS-MAC
- AEC CCM (uses a combination of CTR + CBC-MAC hardware via sotfware drivers)

The AES hardware accelerator can be fed with paintext/ciphertext from either CPU or using DMA. Sustained throughput of one 16 byte ECB block per 23 cycles is possible corresponding to > 30 Mbps.

The CC2340R5 device supports Random Number Generation (RNG) using on-chip analog noise as the nondeterministic noise source for the purpose of generating a seed for a cryptographically secure counter deterministic random bit generator (CTR-DRBG) that in turn is used to generate random numbers for keys, initialization vectors (IVs), and other random number requirements. Hardware acceleration of AES CTR-DRBG is supported.

Together with a large selection of open-source cryptography libraries provided with the Software Development Kit (SDK), this allows for secure and future proof IoT applications to be easily built on top of the platform.

9.6 Timers

A large selection of timers are available as part of the CC2340R5 device. These timers are:

- **Real-Time Clock (RTC)**

  The RTC is a 67-bit, 2-channel timer running on the LFCLK system clock in all power states shutdown power modes or device reset with a software-visible resolution of 8 us and range of 71.4 years. It accumulates time elapsed since reset each LFCLK by a provided period value, LFINC, with a precision of 2^{16} µs. The RTC timer's period value, LFINC has a constant (but overridable) value of exactly 1/32768 s when LFXT sources LFCLK and uses a hardware measurement of LFCLK period when LFOSC sources LFCLK. A hardware synchronization mechanism exists between the system timer (SYSTIM) and the RTC to ensure that the multi-channel and higher resolution SYSTIM remain in synchronization with the RTC’s time base.

  The RTC has two channels: one compare channel and one capture channel and is capable of waking the device out of the standby power state The RTC compare channel is typically used only by system software and only during the standby power state. The power driver provided in the SimpleLink Software Development Kit (SDK) will configure the RTC with the next pending event on SYSTIM before entering standby power state.

  The RTC provides a countdown to the next compare event to power management logic so that it can optionally start functionality with long wakeup times (HFXT especially) early enough in advance that everything is ready when the wakeup event actually occurs.

- **System Timer (SYSTIM)**

  The SYSTIM is a 34-bit, 5-channel wrap-around timer with a per-channel selectable 32b slice with either a 1 us resolution and 1h11m35s range or 250 ns resolution and 17m54s range. All channels support both capture and single-shot compare (posting an event) operation. One channel is reserved for system software, three channels are reserved for radio software and one channel is freely available to user applications.

  For software convenience a hardware synchronization mechanism automatically ensures that the RTC and SYSTIM share a common time base (albeit with different resolutions/spans). Another software convenience feature is that SYSTIM qualifies any submitted compare values so that the timer channel will immediately

trigger if the submitted event is in the immediate past (4.294s with 1 us resolution and 1.049s with 250 ns resolution).

- **General Purpose Timers (LGPT)**

  The CC2340R5 device provides four LGPTs with 3× 16 bit timers and 1× 24 bit timer, all running on up to 48 MHz. The LGPTs support a wide range of features such as:

  – 3 capture/compare channels
  – One-shot or periodic counting
  – Pulse width modulation (PWM)
  – Time counting between edges and edge counting
  – Input filter implened on each of the channels for all timers
  – IR generation feature available on Timer-0
  – Dead band feature available on Timer-1

  The timer capture/compare and PWM signals are connected to IOs via IO controller module (IOC) and the internal timer event connections to CPU, DMA and other peripherals are via the event fabric, which allows the timers to interact with signals such as GPIO inputs, other timers, DMA and ADC. Two LGPTs (2× 16 bit timers) supports quadrature decoder mode to enable buffered decoding of quadrature-encoded sensor signals. The LGPTs are available in device Active and Idle power modes.

- **Watchdog timer**

  The watchdog timer is used to regain control if the system operates incorrectly due to software errors. Upon counter expiry, the watchdog timer resets the device when periodic monitoring of the system components and tasks fails to verify proper functionality. The watchdog timer runs on a 32 kHzclock rate and operates in device active, idle, and standby modes and cannot be stopped once enabled.

9.7 Serial Peripherals and I/O

The CC2340R5 device provides 1xUART, 1xSPI and 1xI2C serial peripherals

The SPI module supports both SPI master and slave up to 12 MHz with configurable phase and polarity.

The UART module implement universal asynchronous receiver and transmitter functions. They support flexible baud-rate generation up to a maximum of 3 Mbps and IRDA SIR mode of operation.

The I2C interface is also used to communicate with devices compatible with the I2C standard. The I2C interface can handle 100 kHz and 400 kHz operation, and can serve as both master and slave.

The I/O controller (IOC) controls the digital I/O pins and contains multiplexer circuitry to allow a set of peripherals to be assigned to I/O pins in a fixed manner over DIOs. All digital I/Os are interrupt and wake-up capable, have a programmable pullup and pulldown function, and can generate an interrupt on a negative or positive edge (configurable). When configured as an output, pins can function as either push-pull, open-drain, or open source. Five GPIOs have high-drive capabilities, which are marked in **bold** in Section 7.

For more information, see the CC23xx SimpleLink™ Wireless MCU Technical Reference Manual.

9.8 Battery and Temperature Monitor

A combined temperature and battery voltage monitor is available in the CC2340R5 device. The battery and temperature monitor allows an application to continuously monitor on-chip temperature and supply voltage and respond to changes in environmental conditions as needed. The module contains window comparators to interrupt the system CPU when temperature or supply voltage go outside defined windows. These events can also be used to wake up the device from Standby mode through the Always-On (AON) event fabric.

9.9 µDMA

The device includes a direct memory access (µDMA) controller. The µDMA controller provides a way to offload data-transfer tasks from the system CPU, thus allowing for more efficient use of the processor and the available bus bandwidth. The µDMA controller can perform a transfer between memory and peripherals. The µDMA

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controller has dedicated channels for each supported on-chip module and can be programmed to automatically perform transfers between peripherals and memory when the peripheral is ready to transfer more data.

Some features of the µDMA controller include the following (this is not an exhaustive list):

- Channel operation of up to 8 channels, with 6 channels having dedicated peripheral interface and 2 channels having ability to be triggered via configurable events.
- Transfer modes: memory-to-memory, memory-to-peripheral, peripheral-to-memory, and peripheral-to-peripheral
- Data sizes of 8, 16, and 32 bits
- Ping-pong mode for continuous streaming of data

9.10 Debug

The on-chip debug support is supported through the Serial Wire Debug (SWD) interface, which is a 2-wire form of the JTAG (IEEE 1149.1) interface. The debug configuration used for the device has 4 HW break-point (address comparators).

9.11 Power Management

To minimize power consumption, the CC2340R5 supports a number of power modes and power management features (see Table 9-1).

Table 9-1. Power Modes

MODE	SOFTWARE CONFIGURABLE POWER MODES (1)				RESET PIN HELD
	ACTIVE	IDLE	STANDBY	SHUTDOWN	
CPU	Active	Off	Off	Off	Off
Flash	On	Available	Off	Off	Off
SRAM	On	On	Retention	Off	Off
Radio	Available	Available	Off	Off	Off
Supply System	On	On	Duty Cycled	Off	Off
CPU register retention	Full	Full	Full (2)	No	No
SRAM retention	Full	Full	Full	Off	Off
48 MHz high-speed clock (HFCLK)	HFXT or HFOSC	HFXT or HFOSC	Off	Off	Off
32 kHz low-speed clock (LFCLK)	LFXT or LFOSC	LFXT or LFOSC	LFXT or LFOSC	Off	Off
Peripherals	Available	Available	IO controller and BATMON	Off	Off
Wake-up on RTC	N/A	Available	Available	Off	Off
Wake-up on pin edge	N/A	Available	Available	Available	Off
Wake-up on reset pin	On	On	On	On	On
Brownout detector (BOD)	On	On	On	On	Off
Power-on reset (POR)	On	On	On	On	Off
Watchdog timer (WDT)	Available	Available	Available or Paused	Off	Off

(1) "Available" indicates that the specific IP or feature can be enabled by user application in the corresponding device operating modes. "On" indicates that the specific IP or feature is turned on irrespective of the user application configuration of the device in the corresponding device operating mode. "Off" indicates that the specific IP or feature is turned off and not available for the user application in the corresponding device operating mode.
(2) Software-based retention of CPU registers with context save and restore when entering and exiting standby power mode

In **Active** mode, the application system CPU is actively executing code. Active mode provides normal operation of the processor and all of the peripherals that are currently enabled. The system clock can be any available clock source (see Table 9-1).

In **Idle** mode, all active peripherals can be clocked, but the system CPU core and no code is executed. DMA access to memories can optionally be enabled in idle mode. Additionally, flash memory can be enabled or disabled based on user configuration. Any interrupt event brings the processor back into active mode.

In **Standby** mode, only the always-on (AON) domain is active. An external wake-up event, RTC event, or comparator event (LP-COMP) is required to bring the device back to active mode. MCU peripherals with retention do not need to be reconfigured when waking up again, and the CPU continues execution from where it went into standby mode. All GPIOs are latched in standby mode.

In **Shutdown** mode, the device is entirely turned off (including the AON domain), and the I/Os are latched with the value they had before entering shutdown mode. A change of state on any I/O pin defined as a *wake from shutdown pin* wakes up the device and functions as a reset trigger. The CPU can differentiate between reset in this way and reset-by-reset pin or power-on reset, or thermal shutdown reset, by reading the reset status register. The only state retained in this mode are the latched I/O state, 3V register bank, and the flash memory contents.

Note

The power, RF and clock management for the CC2340R5 device require specific configuration and handling by software for optimized performance. This configuration and handling is implemented in the TI-provided drivers that are part of the CC2340R5 software development kit (SDK). Therefore, TI highly recommends using this software framework for all application development on the device. The complete SDK with TI-RTOS (optional), device drivers, and examples are offered free of charge in source code.

9.12 Clock Systems

The CC2340R5 device has the following internal system clocks.

The 48 MHz HFCLK is used as the main system (MCU and peripherals) clock. This can be driven by the internal 48 MHz RC Oscillator (HFOSC) or an external 48 MHz crystal (HFXT). Radio operation requires an external 48 MHz crystal.

The 32.768 kHz LFCLK is used as the internal low-frequency system clock. It is used for the RTC, the watchdog timer (if enabled in standby power mode), and to synchronize the radio timer before or after Standby power mode. LFCLK can be driven by the internal 32.8 kHz RC Oscillator (LFOSC), a 32.768 kHz watch-type crystal, or clock input in LFXT bypass mode. When using a crystal or the internal RC oscillator, the device can output the 32 kHz LFCLK signal to other devices, thereby reducing the overall system cost.

9.13 Network Processor

Depending on the product configuration, the CC2340R5 device can function as a wireless network processor (WNP - a device running the wireless protocol stack with the application running on a separate host MCU), or as a system-on-chip (SoC - with the application and protocol stack running on the system CPU inside the device).

In the first case, the external host MCU communicates with the device using SPI or UART. In the second case, the application must be written according to the application framework supplied with the wireless protocol stack.

10 Application, Implementation, and Layout

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

10.1 Reference Designs

The following reference designs should be followed closely when implementing designs using the CC2340R5 device.

Special attention must be paid to RF component placement, decoupling capacitors and DCDC regulator components, as well as ground connections for all of these.

LP-EM-CC2340R5 Design Files	The CC2340R5 LaunchPad Design Files contain detailed schematics and layouts to build application specific boards using the CC2340R5 device.
Sub-1 GHz and 2.4 GHz Antenna Kit for LaunchPad™ Development Kit and SensorTag	The antenna kit allows real-life testing to identify the optimal antenna for your application. The antenna kit includes 16 antennas for frequencies from 169 MHz to 2.4 GHz, including: • PCB antennas • Helical antennas • Chip antennas • Dual-band antennas for 868 MHz and 915 MHz combined with 2.4 GHz The antenna kit includes a JSC cable to connect to the Wireless MCU LaunchPad Development Kits and SensorTags.

ADVANCE INFORMATION

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed as follows.

11.1 Tools and Software

The CC2340R5 device is supported by a variety of software and hardware development tools.

Development Kit

CC2340R5 LaunchPad™ Development Kit	The CC2340R5 LaunchPad™ Development Kit enables development of high-performance wireless applications that benefit from low-power operation. The kit features the CC2340R5 SimpleLink Wireless MCU, which allows you to quickly evaluate and prototype 2.4-GHz wireless applications such as Bluetooth 5 Low Energy, Zigbee and Thread, plus combinations of these. The kit works with the LaunchPad ecosystem, easily enabling additional functionality like sensors, display and more.

Software

SimpleLink™ CC23XX SDK	The SimpleLink CC23XX Software Development Kit (SDK) provides a complete package for the development of wireless applications on the CC23XX family of devices. The SDK includes a comprehensive software package for the CC2340R5 device, including the following protocol stacks: • Bluetooth Low Energy 4 and 5.3 • Zigbee 3.0 • TI 15.4-Stack - an IEEE 802.15.4-based star networking solution for 2.4 GHz The SimpleLink CC23XX SDK is part of TI's SimpleLink MCU platform, offering a single development environment that delivers flexible hardware, software and tool options for customers developing wired and wireless applications. For more information about the SimpleLink MCU Platform, visit https://www.ti.com/simplelink.

ADVANCE INFORMATION

Development Tools

Code Composer Studio™ Integrated Development Environment (IDE)	Code Composer Studio is an integrated development environment (IDE) that supports TI's Microcontroller and Embedded Processors portfolio. Code Composer Studio comprises a suite of tools used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features. The intuitive IDE provides a single user interface taking you through each step of the application development flow. Familiar tools and interfaces allow users to get started faster than ever before. Code Composer Studio combines the advantages of the Eclipse® software framework with advanced embedded debug capabilities from TI resulting in a compelling feature-rich development environment for embedded developers. CCS has support for all SimpleLink Wireless MCUs and includes support for EnergyTrace™ software (application energy usage profiling). A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. Code Composer Studio is provided free of charge when used in conjunction with the XDS debuggers included on a LaunchPad Development Kit.
Code Composer Studio™ Cloud IDE	Code Composer Studio (CCS) Cloud is a web-based IDE that allows you to create, edit and build CCS and Energia™ projects. After you have successfully built your project, you can download and run on your connected LaunchPad. Basic debugging, including features like setting breakpoints and viewing variable values is now supported with CCS Cloud.
IAR Embedded Workbench® for Arm®	IAR Embedded Workbench® is a set of development tools for building and debugging embedded system applications using assembler, C and C++. It provides a completely integrated development environment that includes a project manager, editor, and build tools. IAR has support for all SimpleLink Wireless MCUs. It offers broad debugger support, including XDS110, IAR I-jet™ and Segger J-Link™. A real-time object viewer plugin is available for TI-RTOS, part of the SimpleLink SDK. IAR is also supported out-of-the-box on most software examples provided as part of the SimpleLink SDK. A 30-day evaluation or a 32 KB size-limited version is available through iar.com.
SmartRF™ Studio	SmartRF™ Studio is a Windows® application that can be used to evaluate and configure SimpleLink Wireless MCUs from Texas Instruments. The application will help designers of RF systems to easily evaluate the radio at an early stage in the design process. It is especially useful for generation of configuration register values and for practical testing and debugging of the RF system. SmartRF Studio can be used either as a standalone application or together with applicable evaluation boards or debug probes for the RF device. Features of the SmartRF Studio include: • Link tests - send and receive packets between nodes • Antenna and radiation tests - set the radio in continuous wave TX and RX states • Export radio configuration code for use with the TI SimpleLink SDK RF driver • Custom GPIO configuration for signaling and control of external switches
CCS UniFlash	CCS UniFlash is a standalone tool used to program on-chip flash memory on TI MCUs. UniFlash has a GUI, command line, and scripting interface. CCS UniFlash is available free of charge.

ADVANCE INFORMATION

11.1.1 SimpleLink™ Microcontroller Platform

The SimpleLink microcontroller platform sets a new standard for developers with the broadest portfolio of wired and wireless Arm® MCUs (System-on-Chip) in a single software development environment. Delivering flexible hardware, software and tool options for your IoT applications. Invest once in the SimpleLink software development kit and use throughout your entire portfolio. Learn more on ti.com/simplelink.

11.2 Documentation Support

To receive notification of documentation updates on data sheets, errata, application notes and similar, navigate to the device product folder (CC2340R5). In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

The current documentation that describes the MCU, related peripherals, and other technical collateral is listed as follows.

TI Resource Explorer

TI Resource Explorer	Software examples, libraries, executables, and documentation are available for your device and development board.

Errata

CC2340R5 Silicon Errata	The silicon errata describes the known exceptions to the functional specifications for each silicon revision of the device and description on how to recognize a device revision.

Application Reports

All application reports for the CC2340R5 device are found on the device product folder (CC2340R5).

Technical Reference Manual (TRM)

CC23xx SimpleLink™ Wireless MCU TRM	The TRM provides a detailed description of all modules and peripherals available in the device family.

11.3 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

12.1 Packaging Information

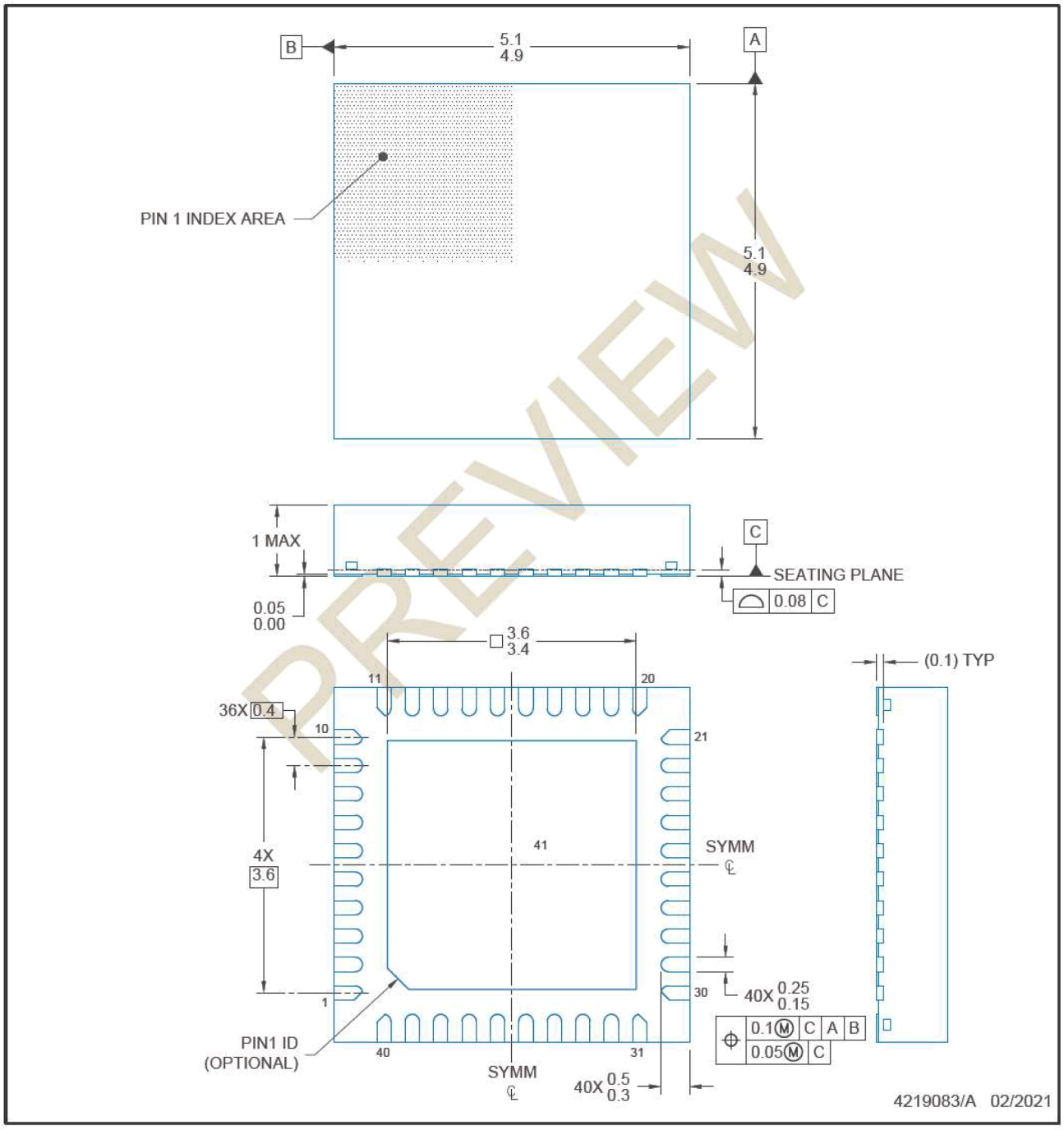
The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGE OUTLINE

RKP0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

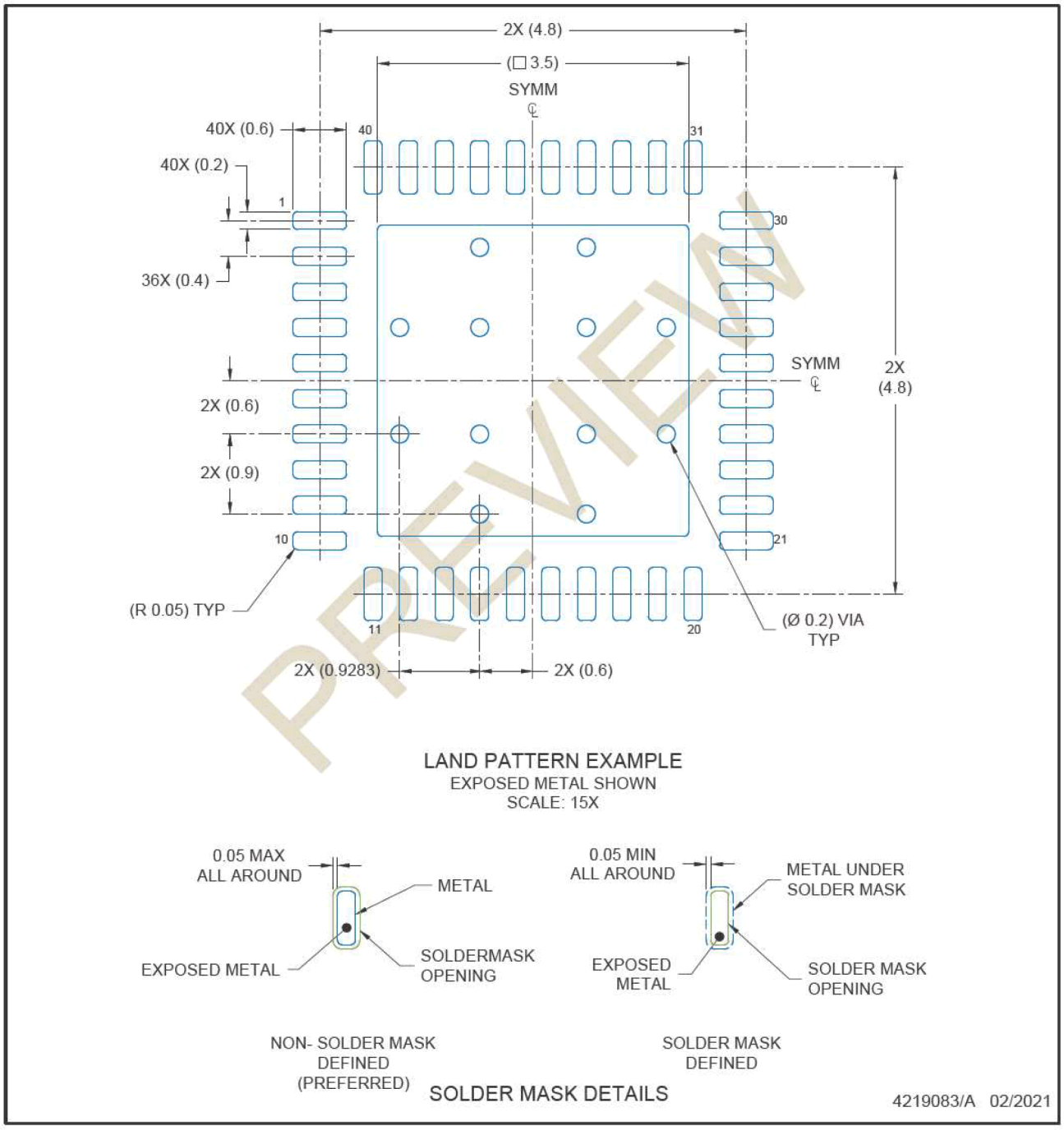
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RKP0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



NOTES: (continued)

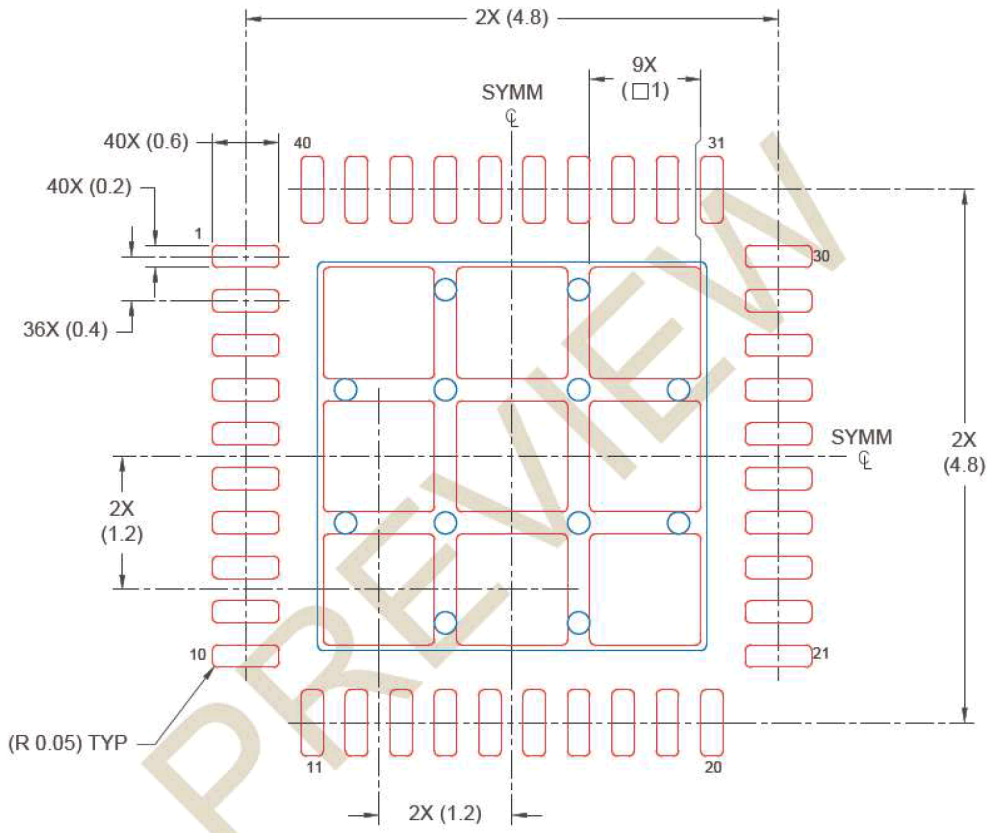
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RKP0040B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK- NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
74% PRINTED COVERAGE BY AREA
SCALE: 15X

4219083/A 02/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

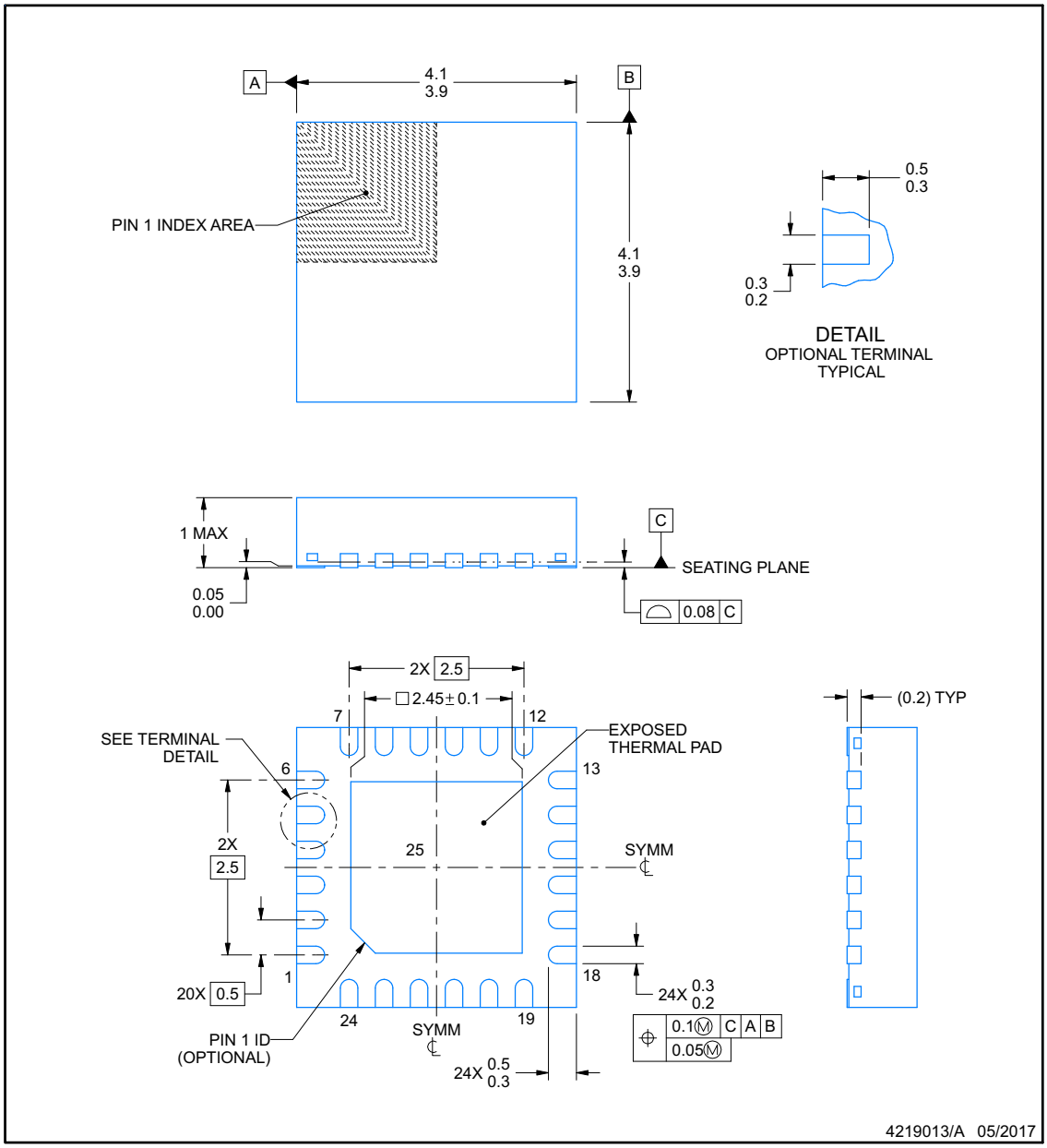
ADVANCE INFORMATION

PACKAGE OUTLINE

RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

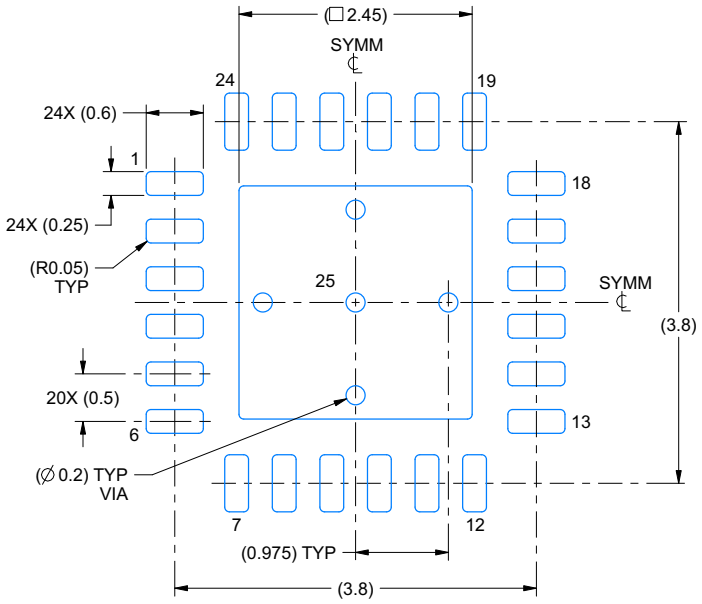
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

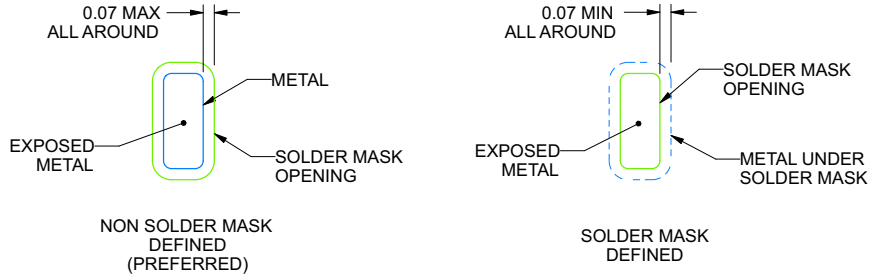
RGE0024B

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

4219013/A 05/2017

NOTES: (continued)

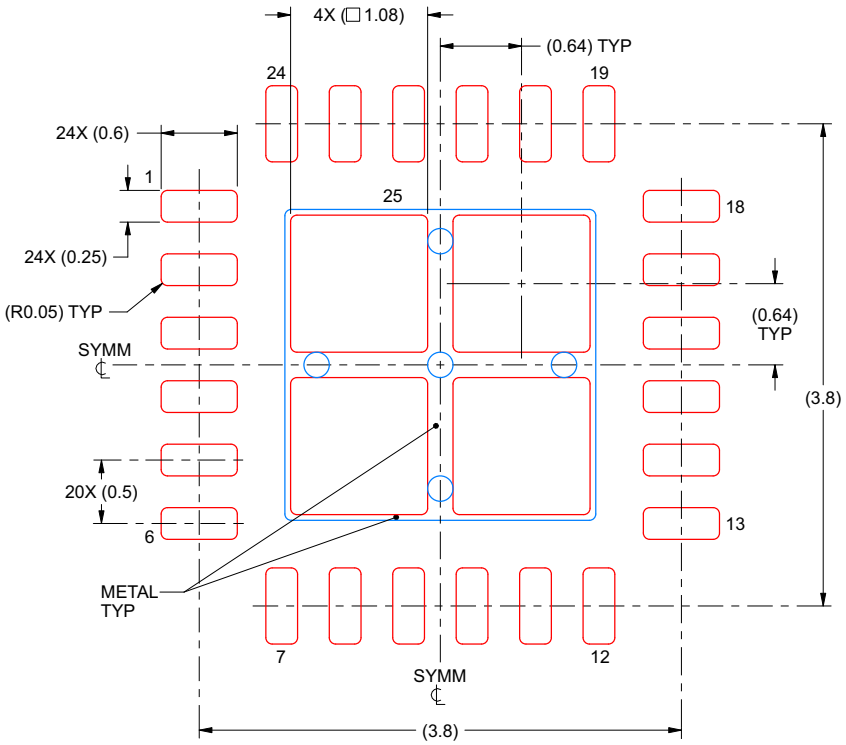
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RGE0024B — **VQFN - 1 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4219013/A 05/2017

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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