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ASR6505 Datasheet

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版本历史

版本号	修改日期	作 者	修 改 说 明
V0.1	2019.3.12	ASR6505 Design Team	Created
V0.2	2019.5.24	ASR6505 Design Team	1. Change the pinmap description. 2. Change chip current parameters.
V0.3	2019.7.1	ASR6505 Design Team	1. Change Product marking of ASR6505.

Table of Contents

1 General Description

The ASR6505 is a general LoRa Wireless Communication Chipset, with integrated LoRa Radio Transceiver, LoRa Modem and an 8-Bit CISC MCU. The MCU uses an advanced STM 8-bit core, with 16MHz operation frequency. The LoRa Radio Transceiver has continuous frequency coverage from 150MHz to 960MHz. The LoRa Modem supports LoRa modulation for LPWAN use cases and (G)FSK modulation for legacy use cases. The LoRa Wireless Communication module designed by ASR6505 provides ultra long range and ultra low power communication for LPWAN application.

The ASR6505 can achieve a high sensitivity of over -140dBm and the maximum transmit power is higher than +21dBm. This makes it suitable to be used in long range LPWAN and have high efficiency. The total chip package is of very small size, 8mm x 8mm, with totally 68 pins.

1.1 Key Feature

- SX1262+STM8L152 integrated.
- Small footprint: 8mm x 8mm x 0.9mm, QFN 68pin.
- LoRa Radio and LoRa Modem.
- Frequency Range: 150MHz ~ 960MHz.
- Maximum Power +21dBm constant RF output.
- High sensitivity: down to -140dBm.
- Deepsleep mode current with RTC: 2uA.
- TX mode current @17dBm: 50mA, @14dBm: 40mA.
- RX mode current: 10mA.
- Programmable bit rate up to 62.5kbps in LoRa modulation mode.
- Programmable bit rate up to 300kbps in (G)FSK modulation mode.
- Preamble detection.
- Embedded memories (up to 64k bytes of Flash memory and 4k bytes of SRAM, 2k bytes of EEPROM).
- 30x configurable GPIOs, 1xI2C, 2xUART, 1xSWIM, 1xSPI, 3xADC.
- LCD driver: 2/4/8 COM, Max 24 Segments.
- 16-MHz Harvard architecture CPU.
- 4-Channel DMA engine.
- Embedded 12-bit 1Msps SAR ADC.
- Embedded 2x12-bit DAC.
- Embedded 2x low power comparators.
- 96-bit unique Chip ID.
- 32.768kHz External Watch Crystal Oscillator.
- 1-16MHz External Crystal Oscillator for MCU (Optional).
- 32MHz External Crystal Oscillator for LoRa Radio.
- Embedded internal Low frequency (38kHz) RC oscillator.
- Most complete EVK demo, with LCD, sensors, debug interfaces on board.

1.2 Block Diagram

Fig. 1.1 shows the block diagram of ASR6505 and the ASR LoRa Communication Module.

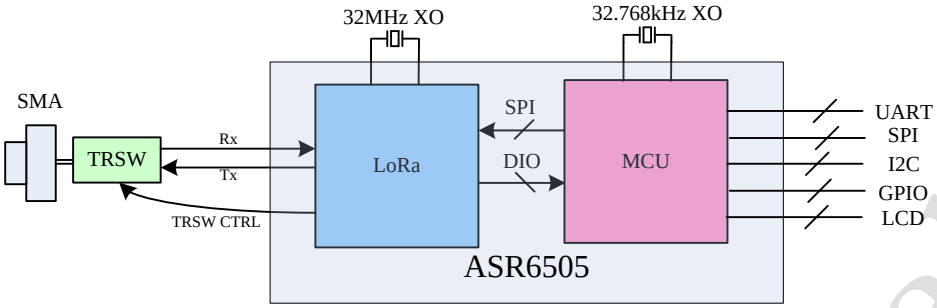


Fig. 1.1: The block diagram of ASR6505 and the ASR LoRa Communication Module

The module of LoRa Communication is designed by ASR6505 and also a reference design for customers. Customers could communicate with ASR6505 by UART/I2C/SPI/LCD and GPIO interfaces.

1.3 General Specification

Following Table 1.1 shows the general specifications of ASR6505 chipset and module.

Table 1.1 General specifications of ASR6505 chipset and module

Chipset Name	ASR6505
Module Name	ASR6505 LoRa Wireless Communication Module
Host Interface	UART, SPI, I2C, GPIO
Operation Conditions	
Temperature	● Storage: -55C ~ +125C ● Operating: -40C ~ +85C
Humidity	● Storage: 5 ~ 95% (Non-Condensing) ● Operating: 10 ~ 95% (Non-Condensing)
Dimension	8mm x 8mm x 0.9mm
Package	QFN Type

2 Electrical Characteristics

Electrical Characteristics include Absolute Maximum Ratings for the Chipset and Module, Recommended Operating Range and Power Consumption Characteristics. All the data are tested under demo board with fully matching and harmonic filtering networks.

2.1 Absolute Maximum Rating

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	-0.3		3.9	V
Vin	Digital Input Voltage Level	-0.3		3.9	V
Pin	RF Input Power			+10	dBm

2.2 Power Consumption Characteristics

Symbol	Parameter	Conditions	Typ.	Max.	Unit
IDD_SL	Supply current in Sleep mode	Without RF Config Retention, without RTC	1		uA
		Without RF Config Retention, with RTC	1.6		
		With RF Config Retention and RTC	2		uA
IDD_RX	Supply current in Receiver mode		9		mA
IDD_TX	Supply current in Transmitter mode	Pout=+22dBm	108		mA
		Pout=+22dBm(TX OPT)	85		mA
		Pout=+21dBm	106		mA
		Pout=+20dBm	98		mA
		Pout=+17dBm	90		mA
		Pout=+17dBm(TX OPT)	50		mA
		Pout=+14dBm	78		mA
		Pout=+14dBm(TX OPT)	40		mA
		Pout=+10dBm	59		mA
		Pout=+5dBm	47		mA

2.3 Recommended Operating Range

Symbol	Parameter	Min.	Typ.	Max.	Unit
VDD	Supply Voltage	1.8	3.3	3.7	V
Pin	RF Input Power			+10	dBm

2.4 RF Characteristics

The table 2.1 gives the electrical specifications for the LoRa RF transceiver operating with LoRa modulation. Following conditions apply unless otherwise specified:

- Supply Voltage = 3.3V.
- Temperature = 25C.
- Frequency bands: 470MHz.
- Bandwidth (BW) = 125kHz.
- Spreading Factor (SF) = 12.
- Coding Rate (CR) = 4/6.
- Package Error Rate (PER) = 1%.
- CRC on payload enabled.
- Payload length = 10bytes.
- Preamble Length = 12 symbols.
- With matched impedances.

Table 2.1: LoRa RF Transceiver Characteristics

LoRa Transmitter RF Characteristics					
Items	Condition	Min.	Typ.	Max.	Unit
Frequency Range		150	470	960	MHz
Tx Power	RFO Pin	18	21	22	dBm

LoRa Receiver RF Characteristics					
Items	Condition	Min.	Typ.	Max.	Unit
Frequency Range		150	470	960	MHz
Sensitivity	125kHz Bandwidth, SF=7		-126		dBm
	125kHz Bandwidth, SF=10		-135		dBm
	125kHz Bandwidth, SF=12		-140		dBm
2nd order harmonic	Tx Power = 20dBm		-41		dBm

2.5 Digital Characteristics

2.5.1 DC Characteristics

Symbol	Description	Conditions	Min.	Typ.	Max.	Unit
VIH	I/O input high level		0.7xVDD			V
VIL	I/O input low level				0.3xVDD	V
RPU	Weak pull up resistor	Vin=GND	30	45	60	KΩ
RPD	Weak pull down resistor	Vin=VDD	30	45	60	KΩ

2.5.2 RST Characteristics

Fig. 2.1 shows the recommended XRES pin connection. An external RESET button is used to generate reset pulse of the whole chip. The 0.1uF capacitor is to filter out the parasitic reset glitch.

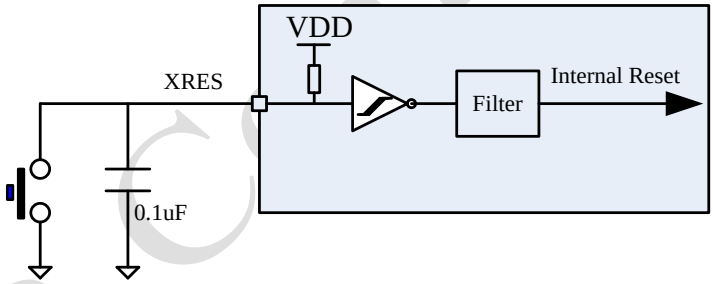


Fig. 2.1: XRES Pin Connection

3 Pin Definition

NO.	PIN_NAME	P/G/I/O	Description
1	VR_PA	O	Regulated power amplifier supply
2	VDD_IN	P	Input voltage for power amplifier, VR_PA
3	GND_PLL	G	Ground
4	XTA	I	XO32M for LoRa input
5	XTB	I	XO32M for LoRa input
6	NC	NC	NC
7	DIO3	I/O	Multipurpose digital I/O-external TCXO32M supply voltage
8	VREG	O	Regulated output voltage from the internal LDO/DC-DC
9	GND_DCC	G	Ground
10	DCC_SW	O	DC-DC Switcher Output
11	VBAT_RF	P	Supply for the LoRa Radio

12	VBAT_DIO	P	Digital I/O supply voltage
13	DIO2	I/O	Multipurpose digital I/O-RF switch control
14	SWIM	I/O	SWIM download pin
15	NRST	I/O	External reset pin
16	LCD_COM0	I/O	LCD Common pin 0
17	LCD_COM1	I/O	LCD Common pin 1
18	LCD_COM2	I/O	LCD Common pin 2
19	VDDA	P	Power supply for MCU analog section
20	VREFP	I	VREFP for ADC
21	UART1_RX	I/O	UART1 RX pin, wake up UART.
22	UART1_TX	I/O	UART1 TX pin, wake up UART.
23	VLCD	I	VLCD voltage input
24	LCD_SEG0	I/O	LCD Segment pin 0
25	LCD_SEG1	I/O	LCD Segment pin 1
26	LCD_SEG2	I/O	LCD Segment pin 2
27	LCD_SEG3	I/O	LCD Segment pin 3
28	LCD_COM3	I/O	LCD Common pin 3
29	LCD_SEG4	I/O	LCD Segment pin 4
30	LCD_SEG5	I/O	LCD Segment pin 5
31	UART0_RX	I	UART0 RX pin, wake up UART.
32	UART0_TX	I	UART0 TX pin, wake up UART.
33	VDDD1	P	Power supply for MCU digital section
34	LCD_SEG6	I/O	LCD Segment pin 6
35	LCD_SEG7	I/O	LCD Segment pin 7
36	LCD_SEG8	I/O	LCD Segment pin 8
37	LCD_SEG9	I/O	LCD Segment pin 9
38	VDDD2	P	Power supply for MCU digital section
39	SPI_MISO	I	SPI slave output, can be external SPI
40	SPI_MOSI	I	SPI slave input, can be external SPI
41	SPI_SCK	I	SPI clock, can be external SPI
42	SPI_NSS	I	SPI slave select, can be external SPI
43	LCD_SEG10	I/O	LCD Segment pin 10
44	LCD_SEG11	I/O	LCD Segment pin 11
45	LCD_SEG12	I/O	LCD Segment pin 12
46	LCD_SEG13	I/O	LCD Segment pin 13
47	LCD_SEG14	I/O	LCD Segment pin 14
48	LCD_SEG15	I/O	LCD Segment pin 15
49	LCD_SEG16	I/O	LCD Segment pin 16
50	GPIO1	I/O	SPI2 NSS
51	GPIO0	I/O	MCU GPIO
52	LCD_SEG17	I/O	LCD Segment pin 17
53	I2C_SDA	I/O	I2C SDA pin
54	I2C_SCL	I/O	I2C SCL pin

55	VDDD3	P	Power supply for MCU digital section
56	ADC1_IN0	I	ADC input pin0
57	ADC1_IN1	I	ADC input pin1
58	GPIO2	I/O	MCU GPIO
59	OSC32K_IN	I	XO32K for MCU input
60	OSC32K_OUT	I	XO32K for MCU input
61	ADC1_IN2	I	ADC input pin3
62	GPIO3	I/O	MCU GPIO
63	GPIO4	I/O	MCU GPIO
64	NSS	I/O	SPI NSS pin for LoRa, should be connected with a MCU SPI NSS externally, for example GPIO1(SPI2_NSS).
65	SCAN	I/O	LoRa Scan pin
66	RFI_P	I	RF receiver input
67	RFI_N	I	RF receiver input
68	RFO	O	RF transmitter output

3.1 Pin Assignment

Fig. 3.1 shows the pin assignment of ASR6505, QFN 8mm x 8mm package is used and the total footprint is 68 pins.

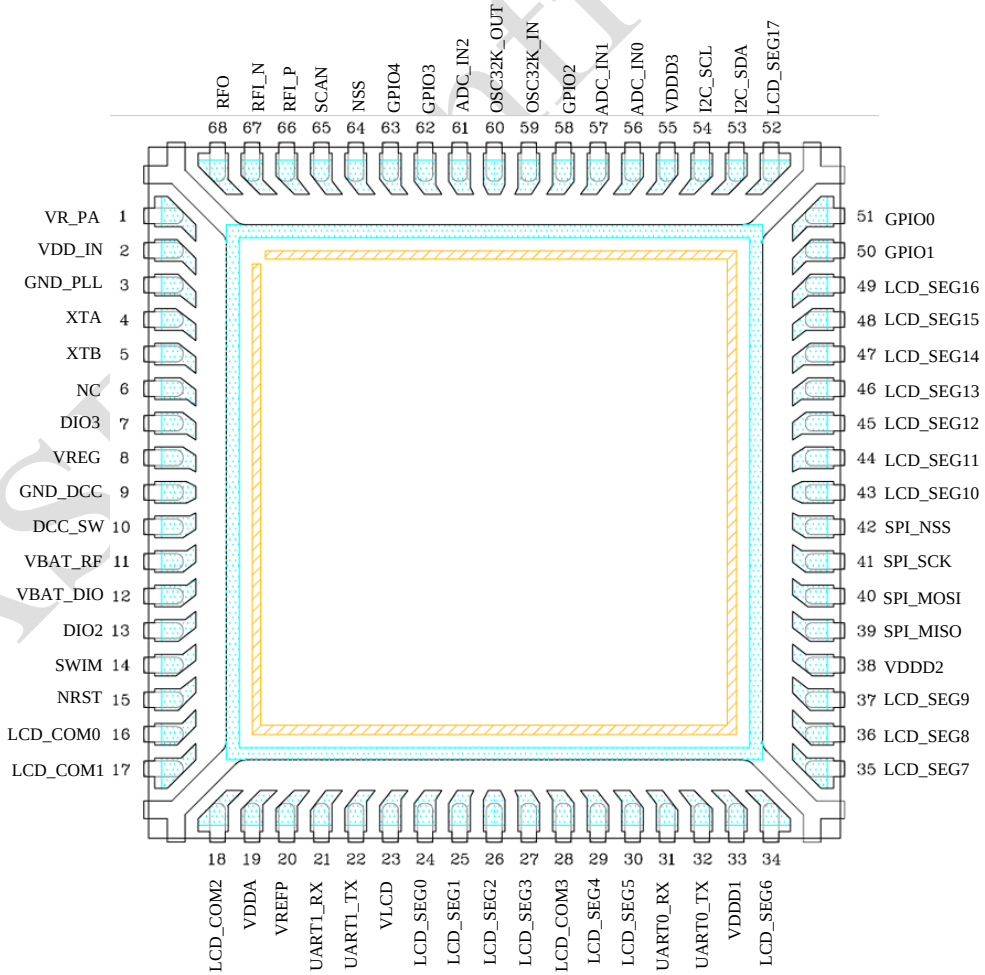
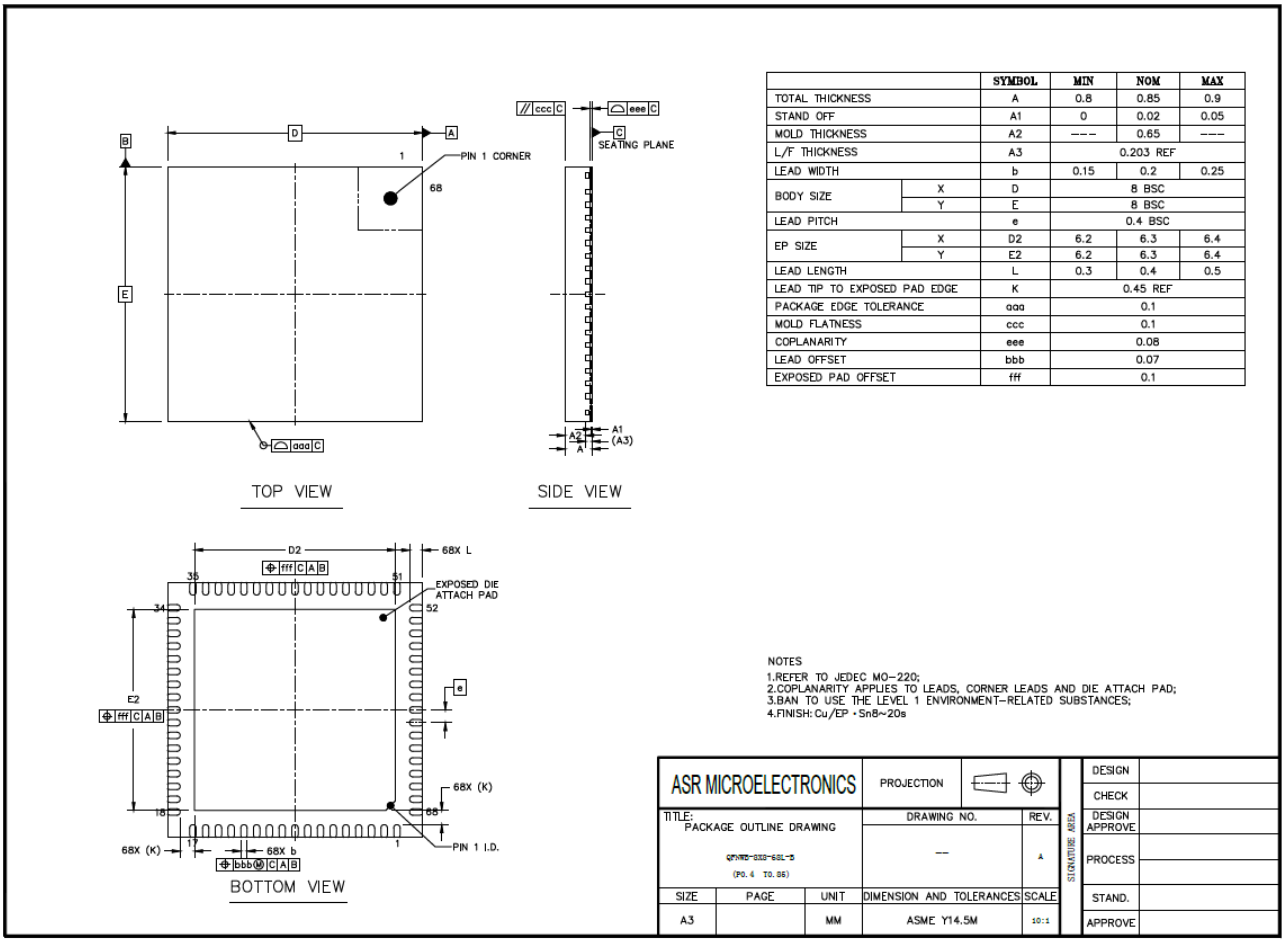


Fig. 3.1 Pin assignment of ASR6505

4 Mechanical Dimension



		SYMBOL	MIN	NOM	MAX
TOTAL THICKNESS		A	0.8	0.85	0.9
STAND OFF		A1	0	0.02	0.05
MOLD THICKNESS		A2	---	0.65	---
L/F THICKNESS		A3		0.203 REF	
LEAD WIDTH		b	0.15	0.2	0.25
BODY SIZE	X	D		8 BSC	
	Y	E		8 BSC	
LEAD PITCH		e		0.4 BSC	
EP SIZE	X	D2	6.2	6.3	6.4
	Y	E2	6.2	6.3	6.4
LEAD LENGTH		L	0.3	0.4	0.5
LEAD TIP TO EXPOSED PAD EDGE		K		0.45 REF	
PACKAGE EDGE TOLERANCE		aaa		0.1	
MOLD FLATNESS		ccc		0.1	
COPLANARITY		eee		0.08	
LEAD OFFSET		bbb		0.07	
EXPOSED PAD OFFSET		fff		0.1	

5 Package Information

5.1 Product Marking

Fig. 5.1 shows the product marking of ASR6505.

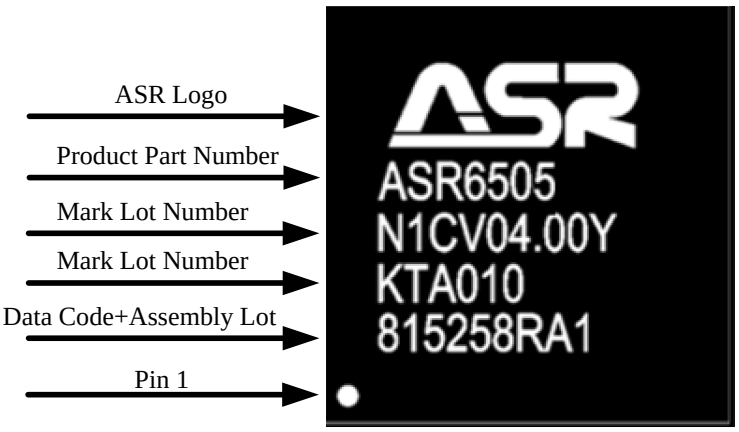


Fig. 5.1 The product marking of ASR6505